

# JITR1/R2\_DDR3

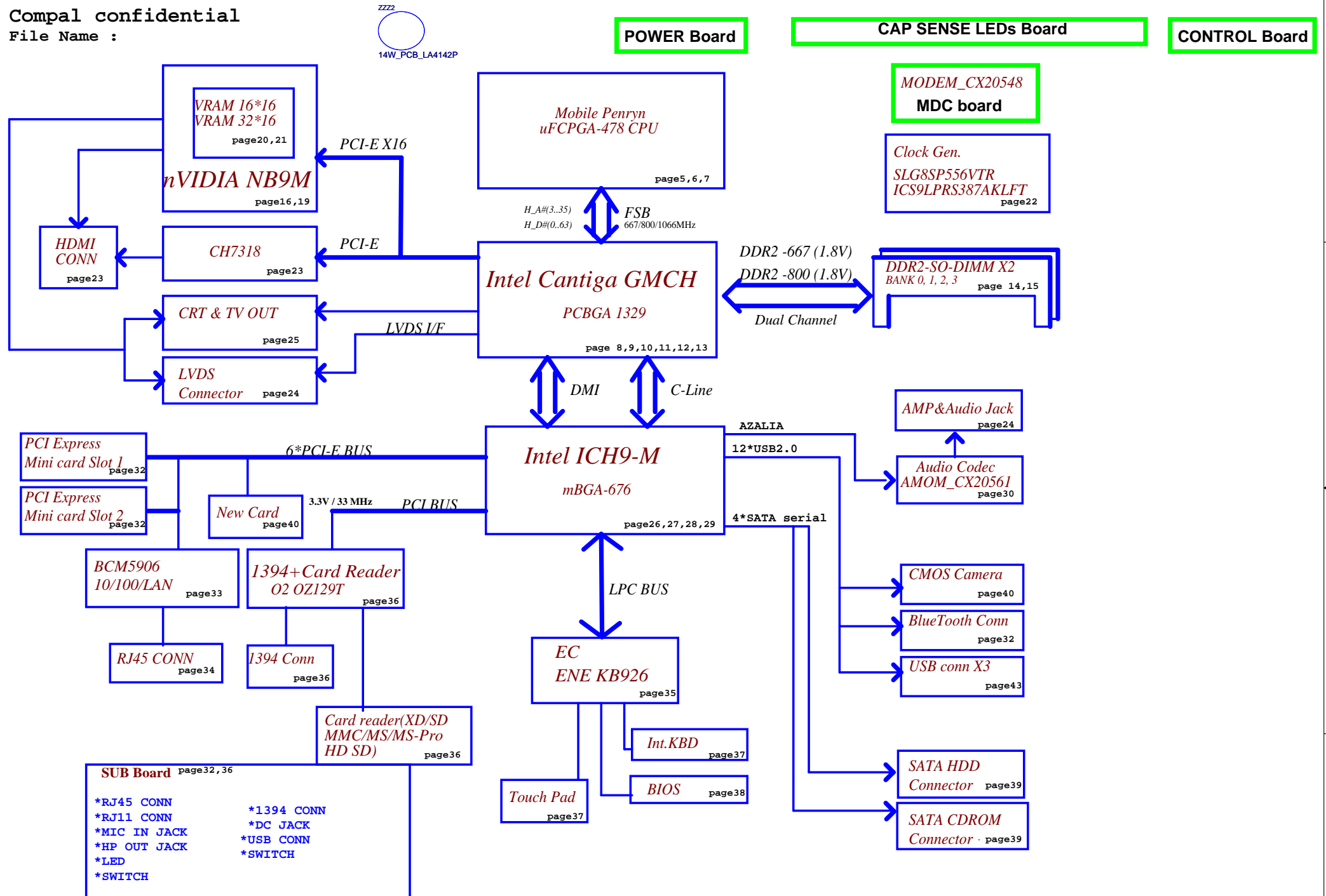
## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_GM/PM+ICH9-M core logic

Friday, April 18, 2008

REV:1.0

Security Classification	Compal Secret Data			Title		
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MB Block Diagram

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DDR2 Voltage Rails

power plane State	+B	+5VALW  +3VALW	+1.8V	+5VS +3VS +1.5VS <b>+0.9VS</b> +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

DDR3 Voltage Rails

power plane State	+B	+5VALW  +3VALW	+1.5V	+5VS +3VS +1.5VS <b>+0.75V</b> +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	V	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICKL_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

VGA and DDR2 Voltage Rails (NB9M-GS)

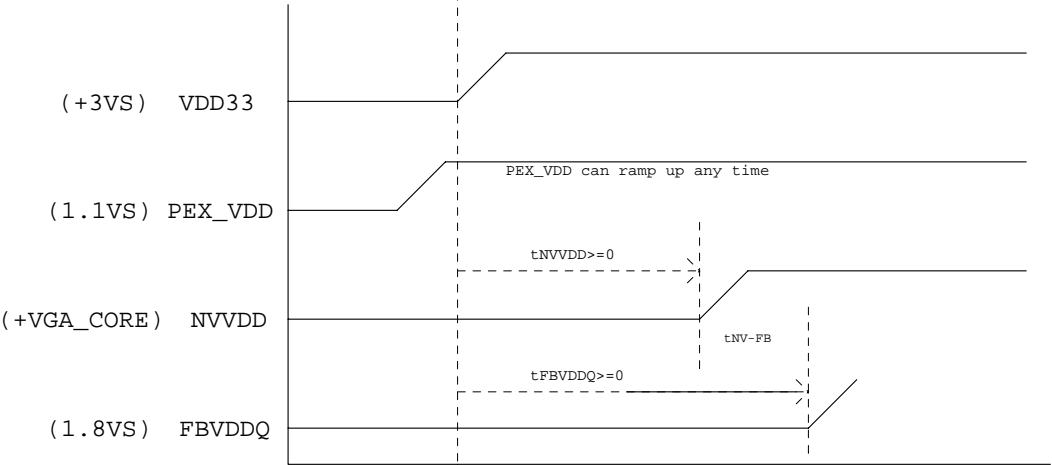
power plane State			+1.8V	+3VS +VGA_CORE
	S0	O	O	O
	S1	O	O	O
	S3	O	O	X
	S5 S4/AC	O	O	X
	S5 S4/ Battery only	O	X	X
	S5 S4/AC & Battery don't exist	X	X	X

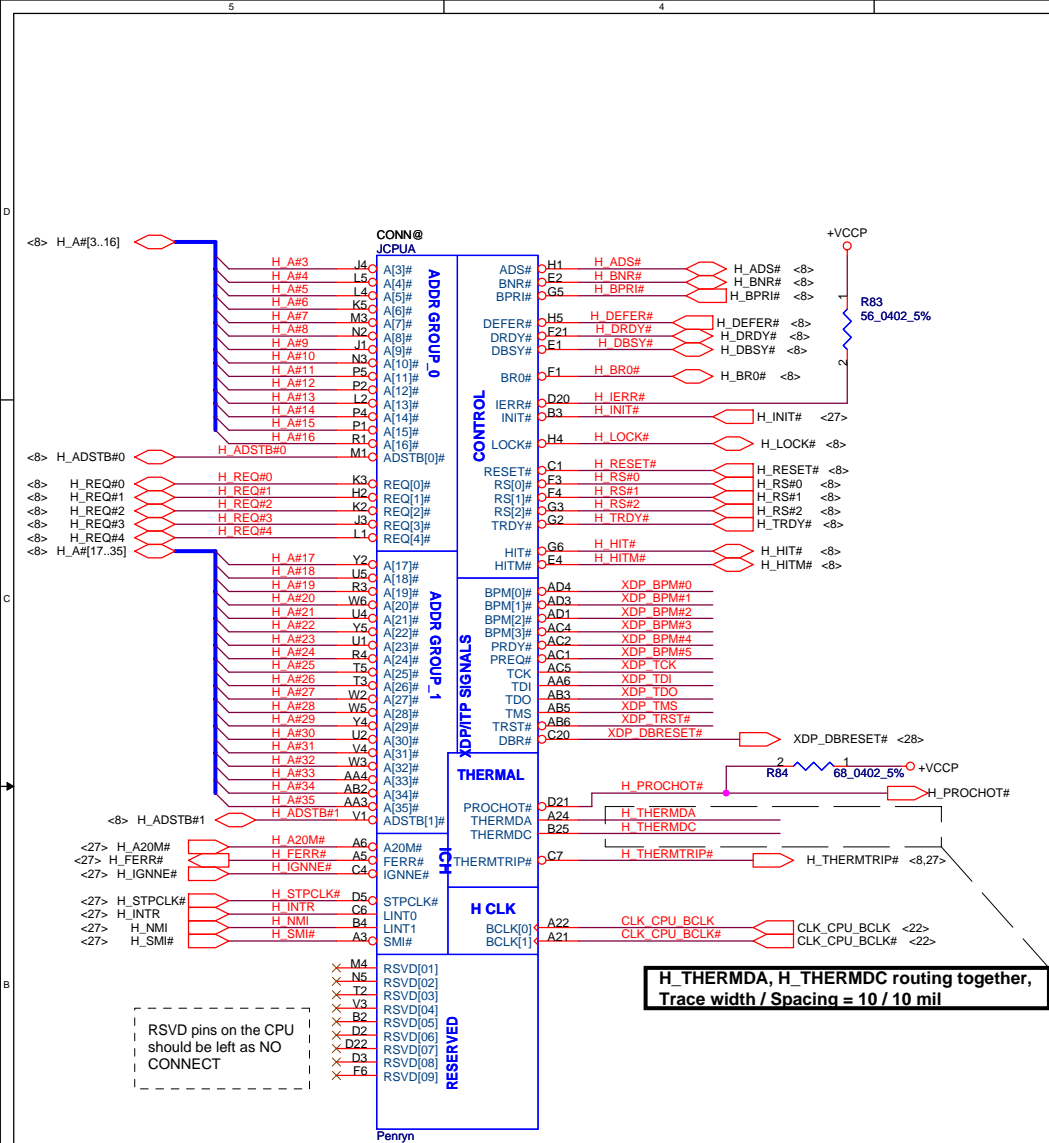
EDP at Tj = 97C\*

Power Supply Rail		NB9M-GS		NB9M-GE	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDD/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

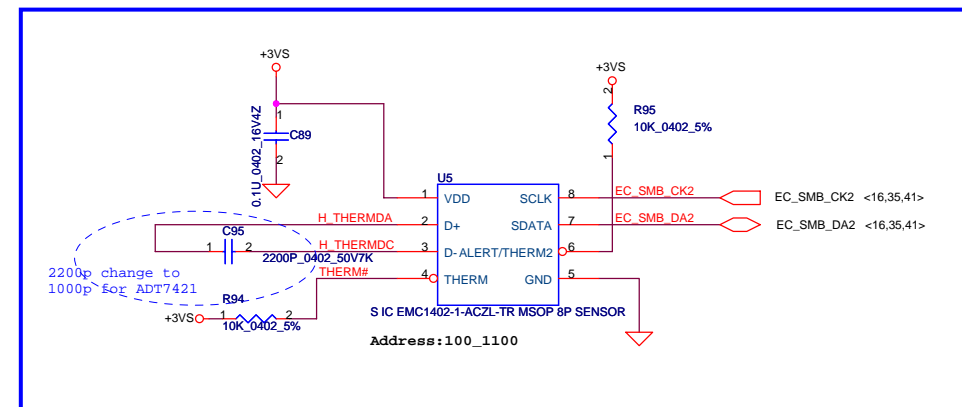
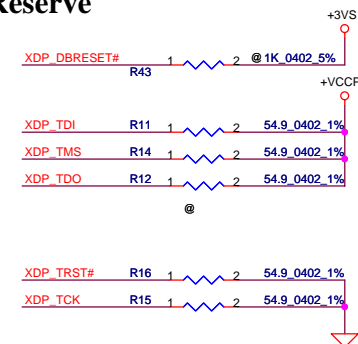
POWER SQUENCE

The ramp time for any rail must be more than 40us

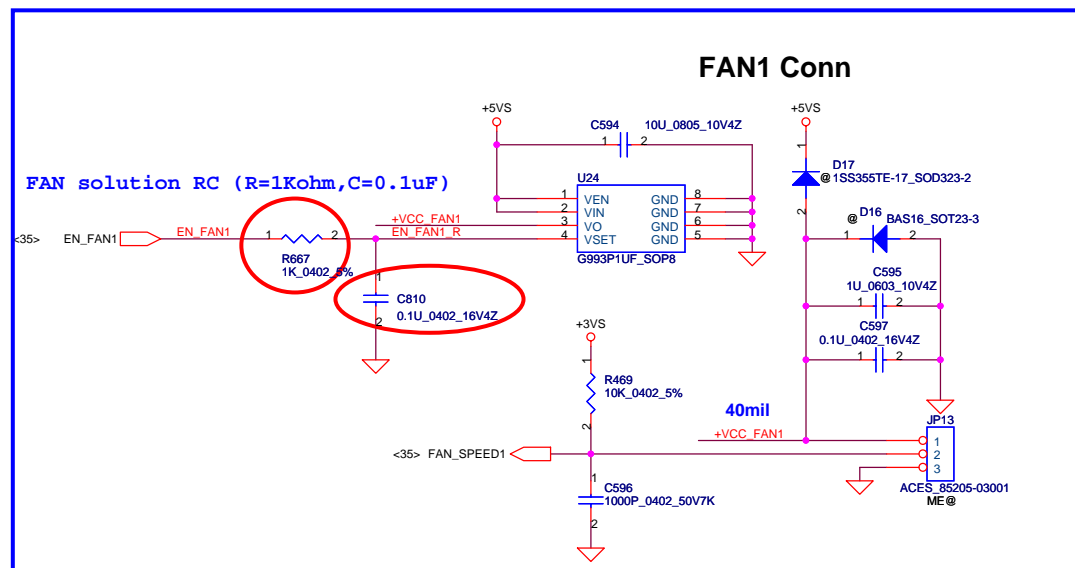




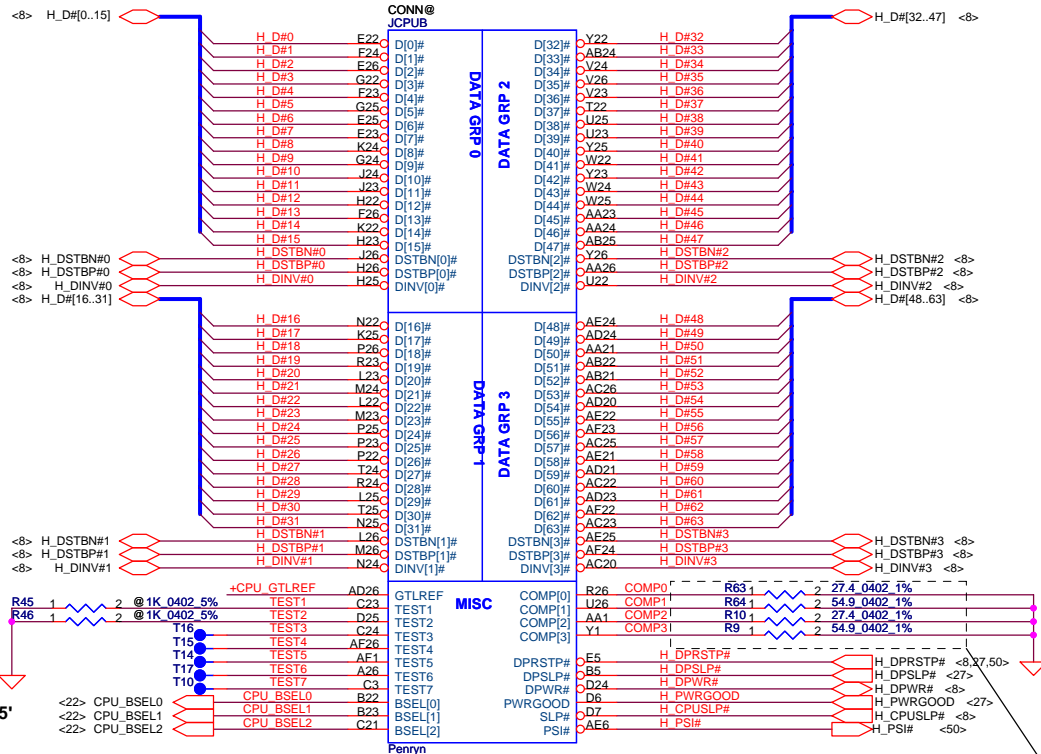
## XDP Reserve



## FAN1 Conn

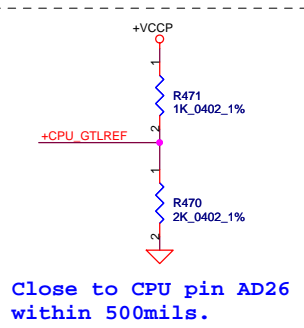


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Width=4 mil ,  
Spacing: 15mil  
(55Ohm)

Layout note: Z0=55 ohm  
0.5" max for GTLREF.

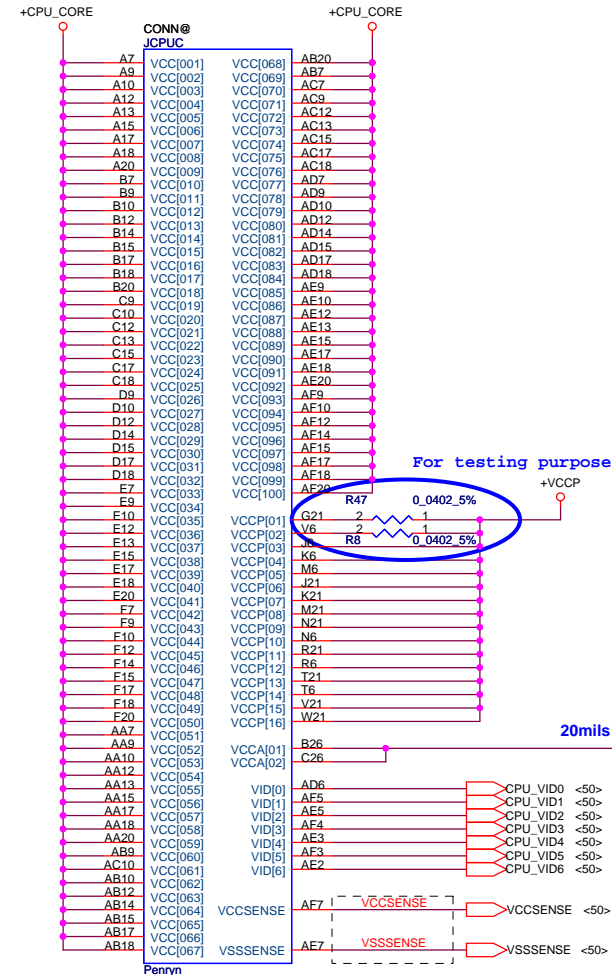


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

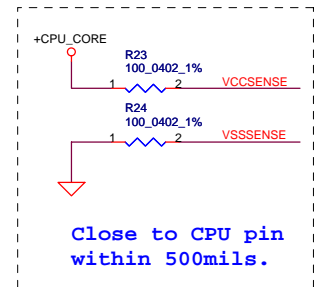
TRACE CLOSELY CPU < 0.5"

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)  
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)



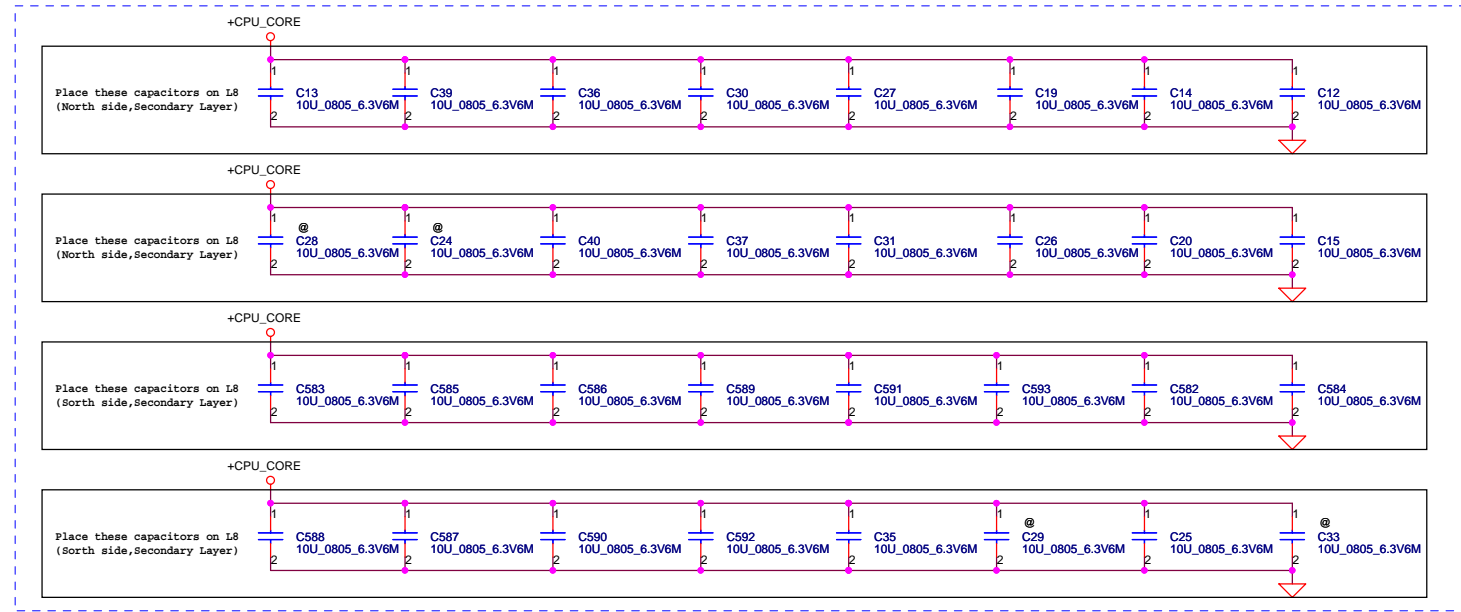
Length match within 25 mils.  
The trace width/space/other is  
16/7/25.

Layout Note:  
Route VCCSENSE and VSSSENSE traces at  
27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.

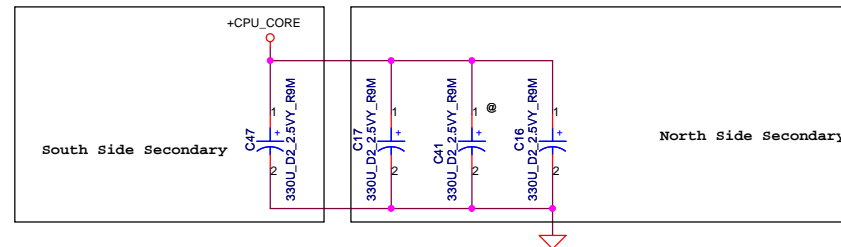


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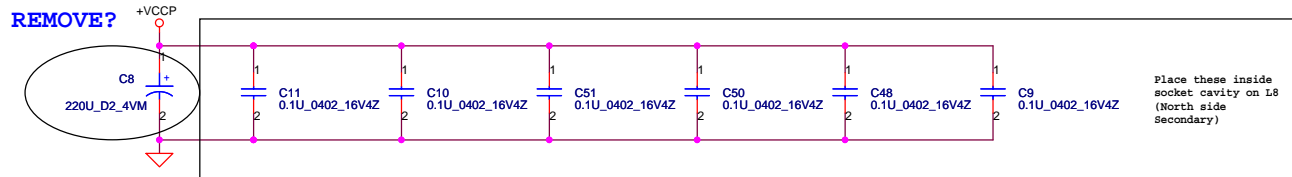
CONN@JCPUD		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D16	VSS[031]	AA11
D19	VSS[032]	AA14
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB16
E24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	AF6
M22	VSS[075]	AF8
M25	VSS[076]	AF11
N1	VSS[077]	AF13
N4	VSS[078]	AF16
N23	VSS[079]	AF19
N26	VSS[080]	AF21
P3	VSS[081]	A25
	VSS[162]	AF25
	VSS[163]	



Mid Frequency Decoupling



ESR <= 1.5m ohm  
Capacitor > 1980uF



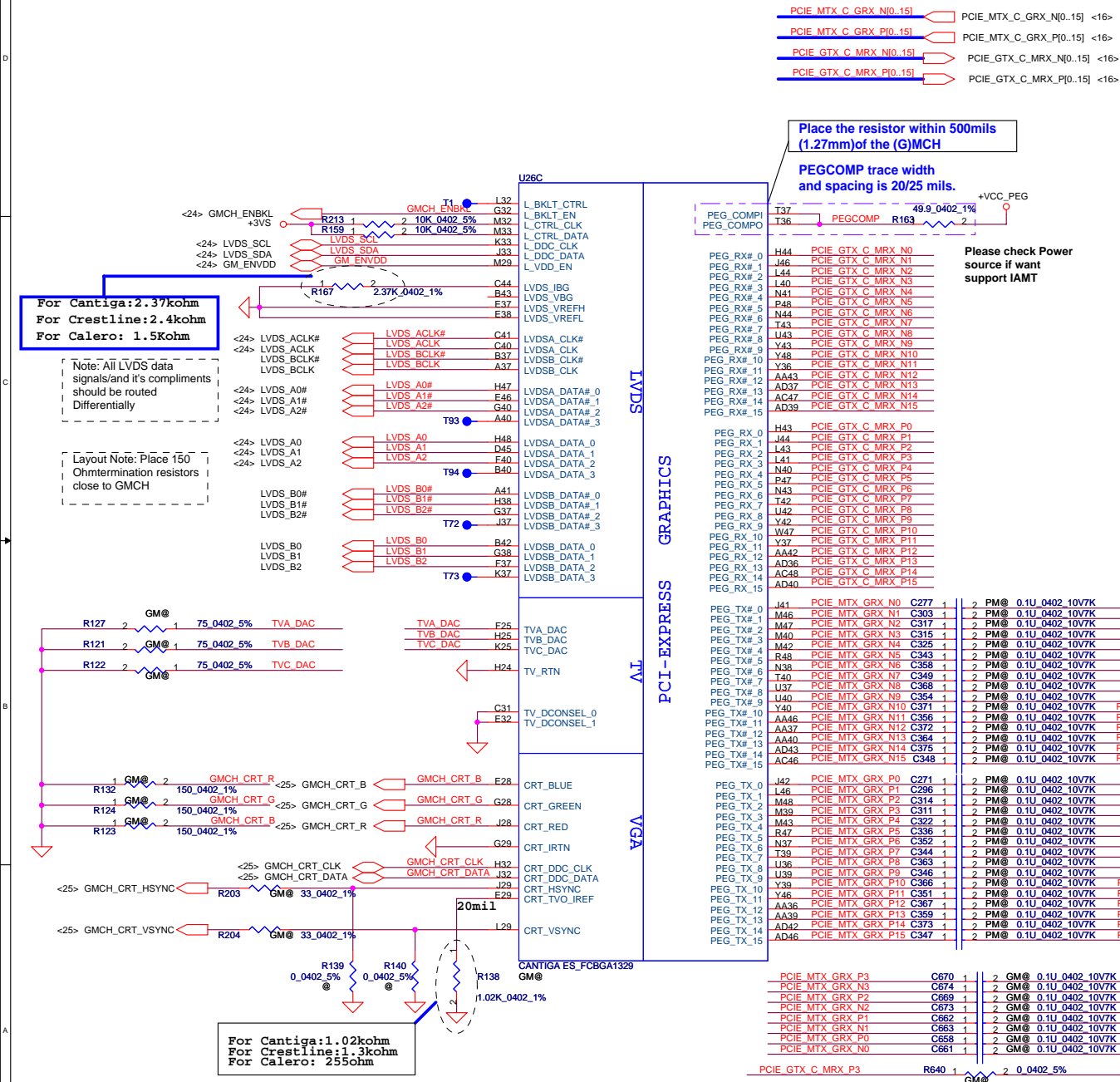
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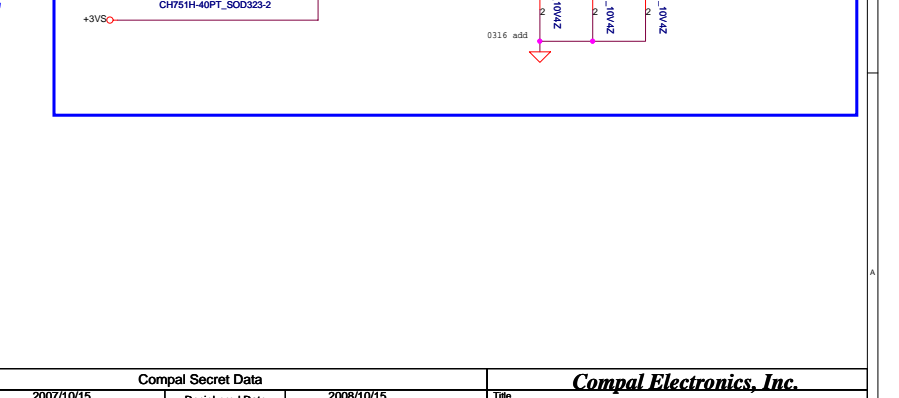
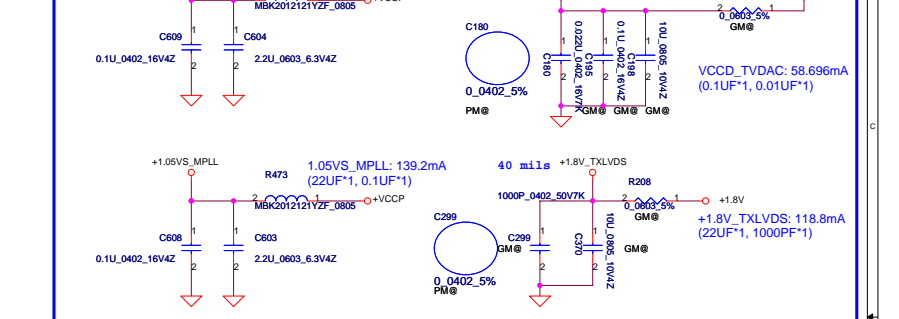
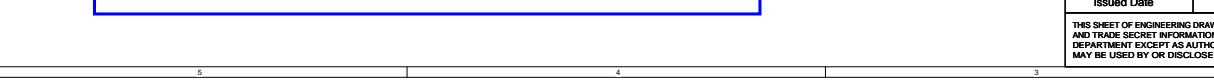
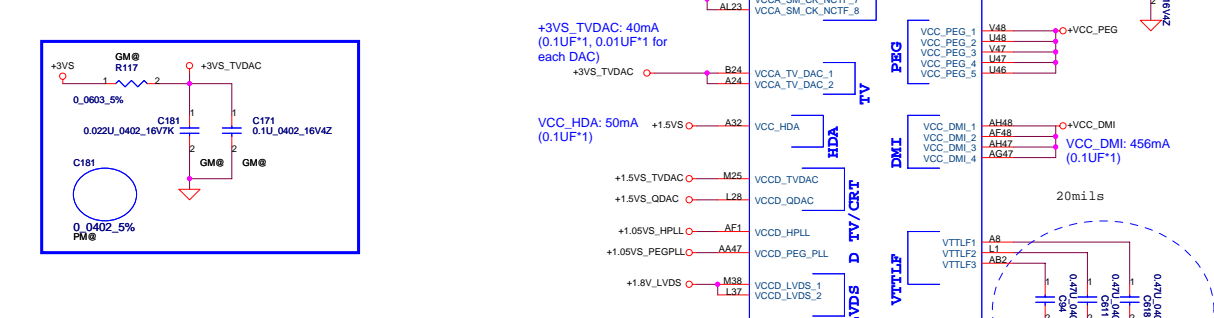
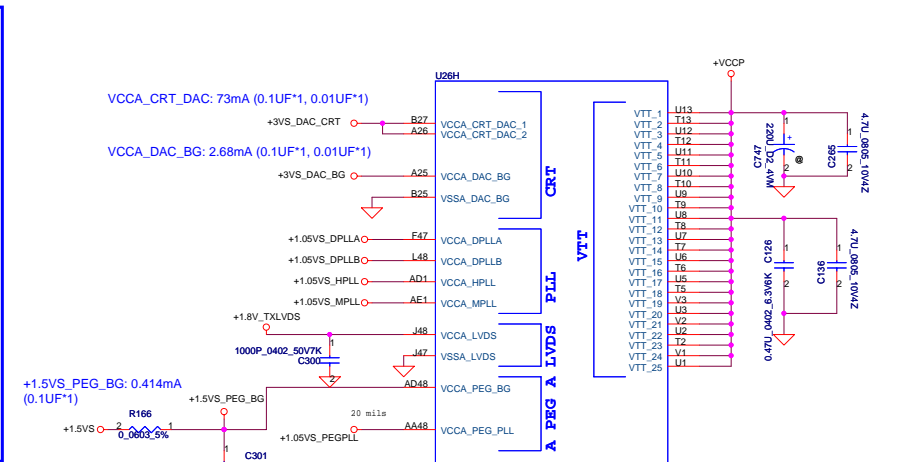


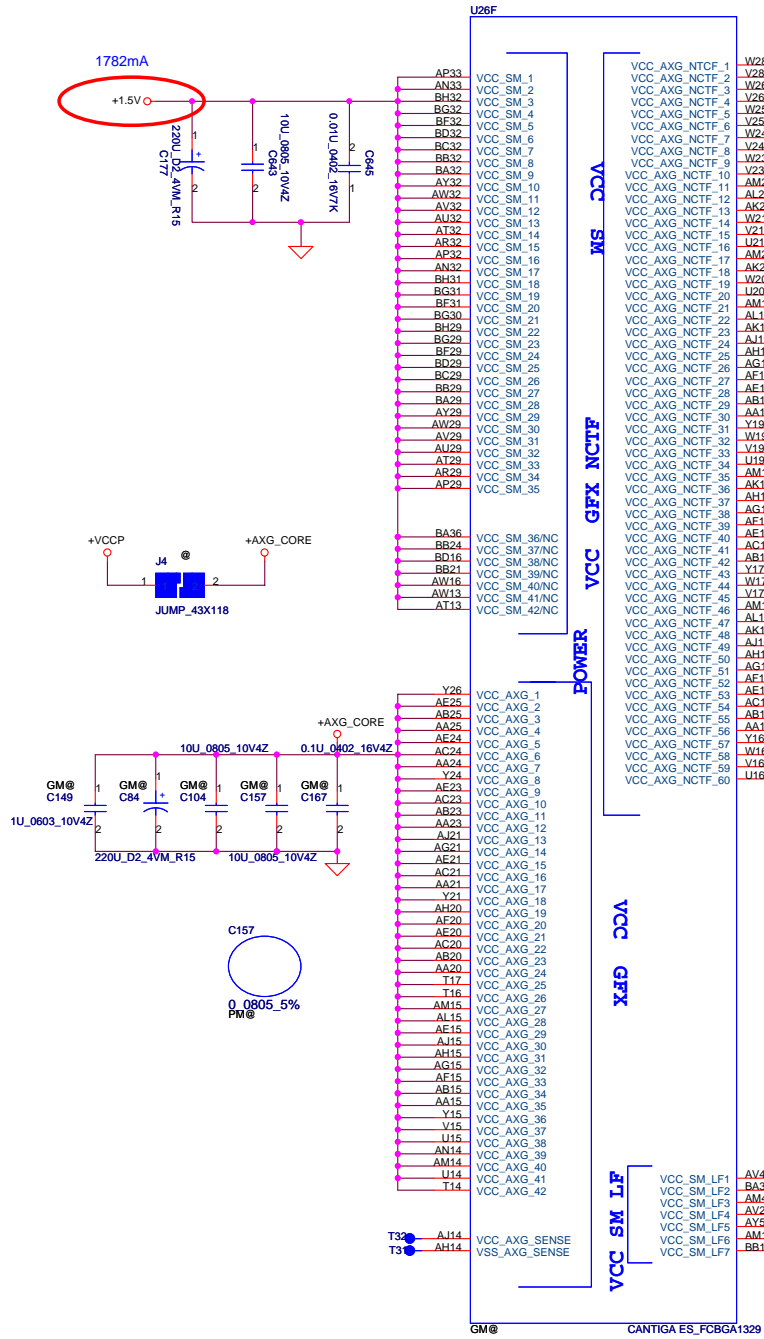
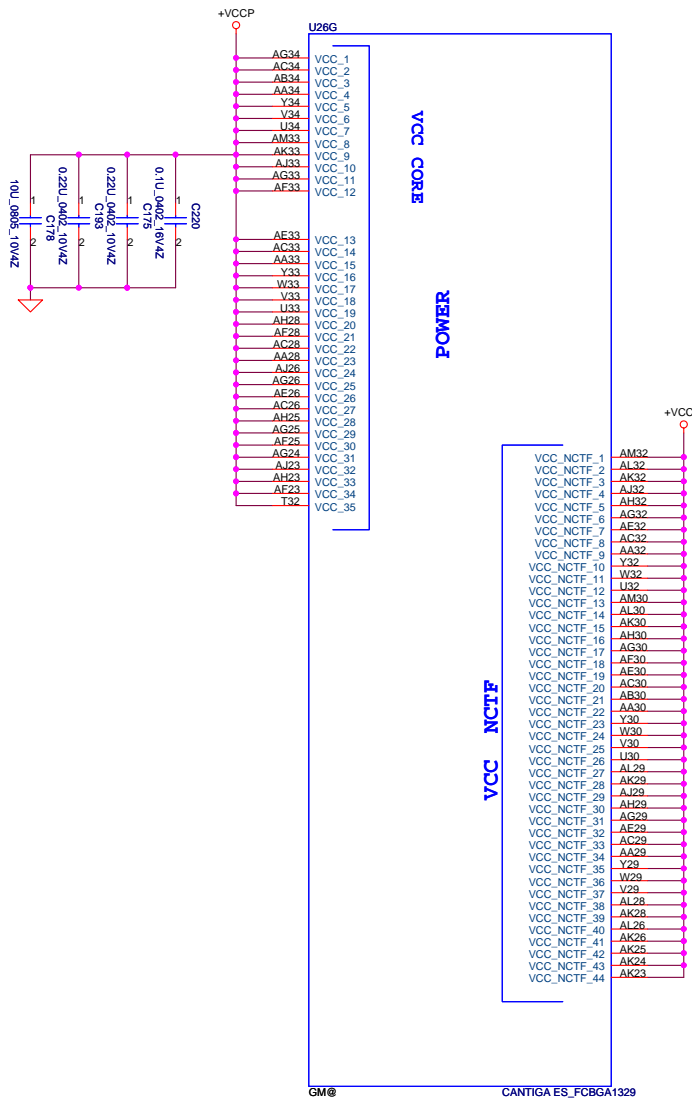


## Strap Pin Table

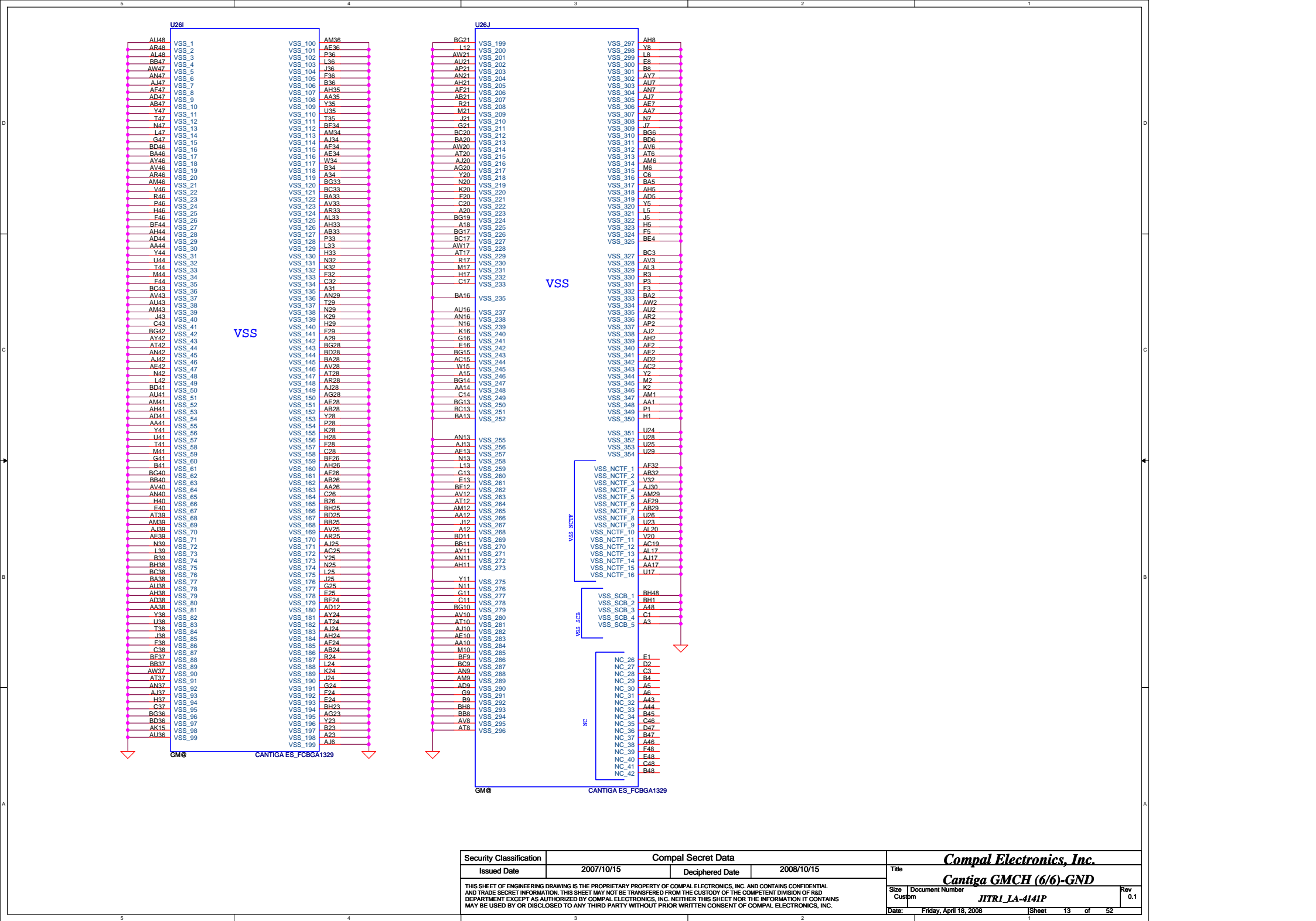
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chipset suite with no confidentiality 1=(TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *







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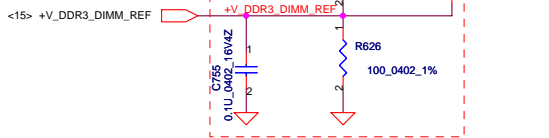
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<9> DDR\_A\_D[0..63]

<9> DDR\_A\_DM[0..7]

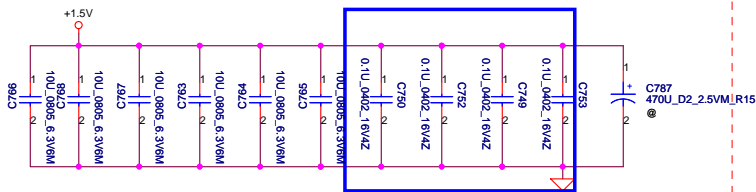
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<9> DDR\_A\_MA[0..14]

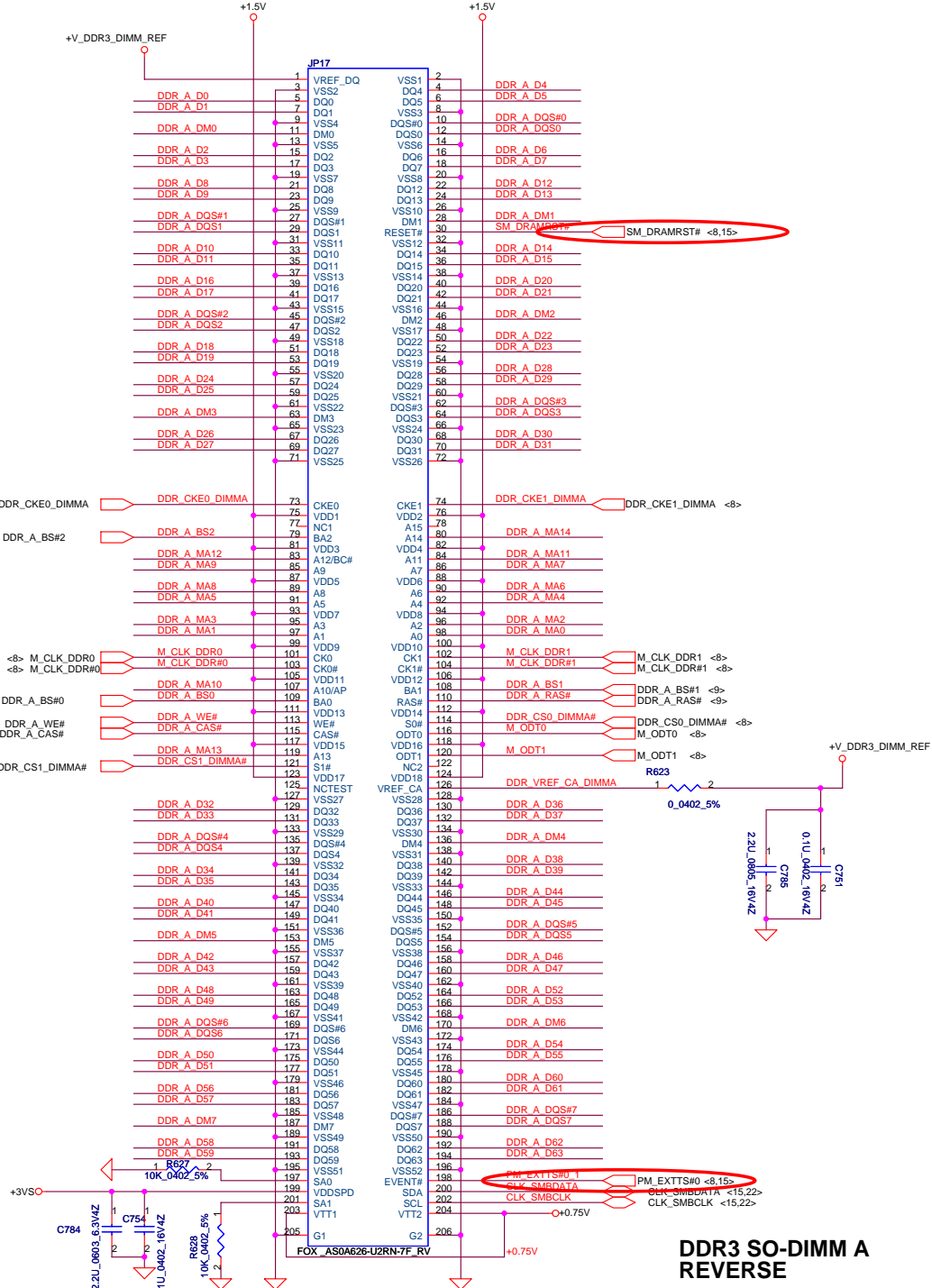
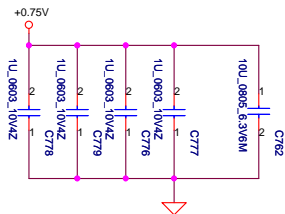


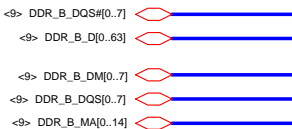
Layout Note:  
Place near JP4

Layout Note: Place these 4 Caps near Command  
and Control signals of DIMM



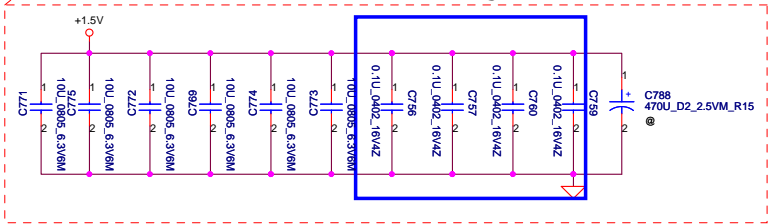
Layout Note:  
Place near JP4.203 & JP4.204



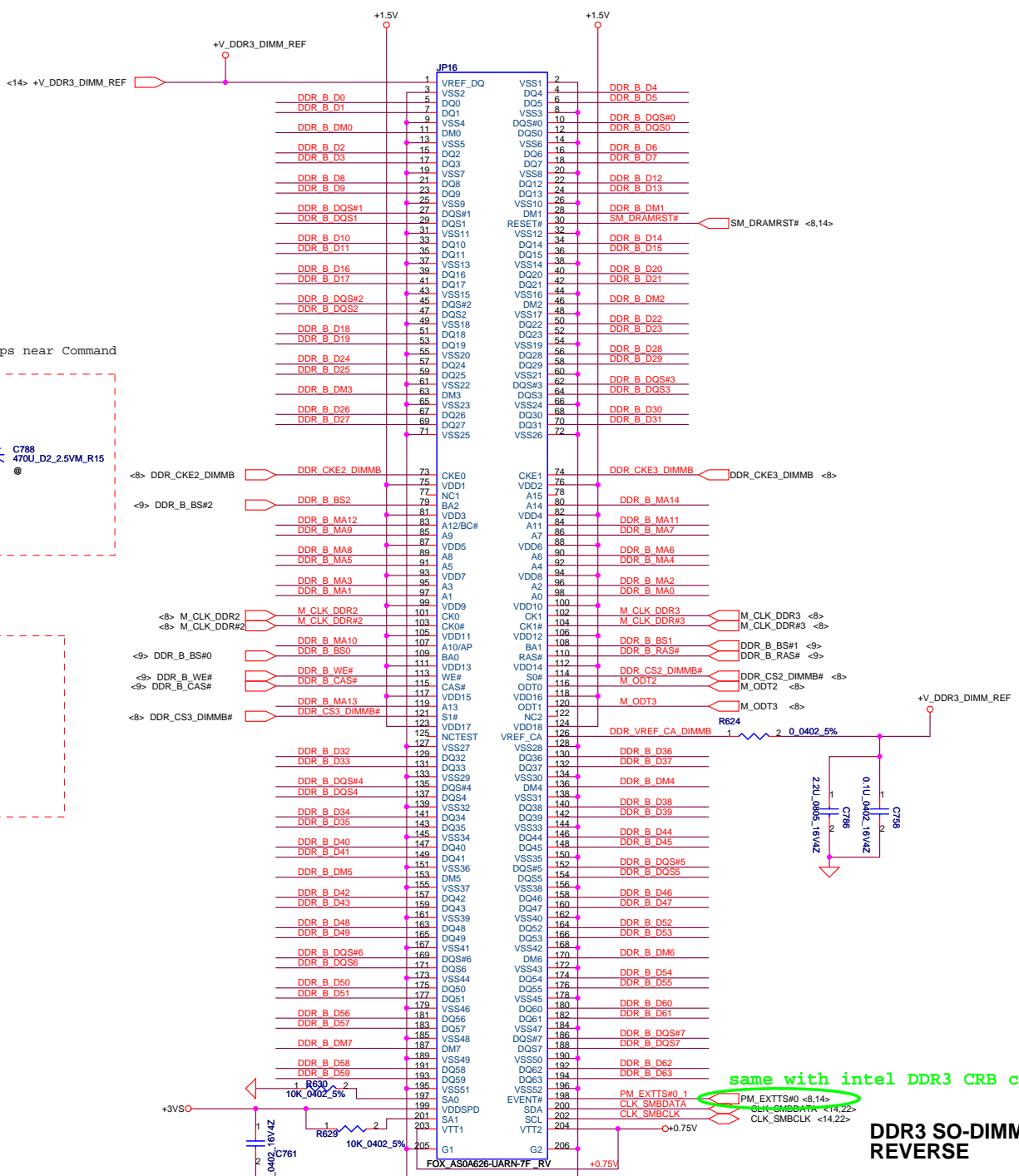
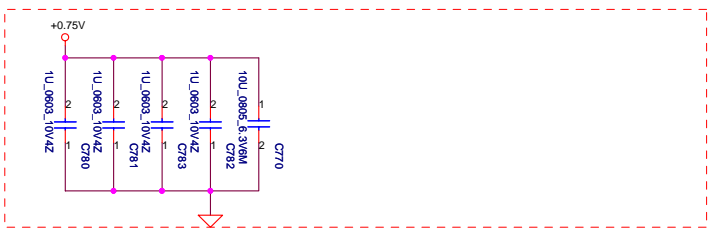


Layout Note:  
Place near JP5

Layout Note: Place these 4 Caps near Command  
and Control signals of DIMM



Layout Note:  
Place near JP5.203 & JP5.204

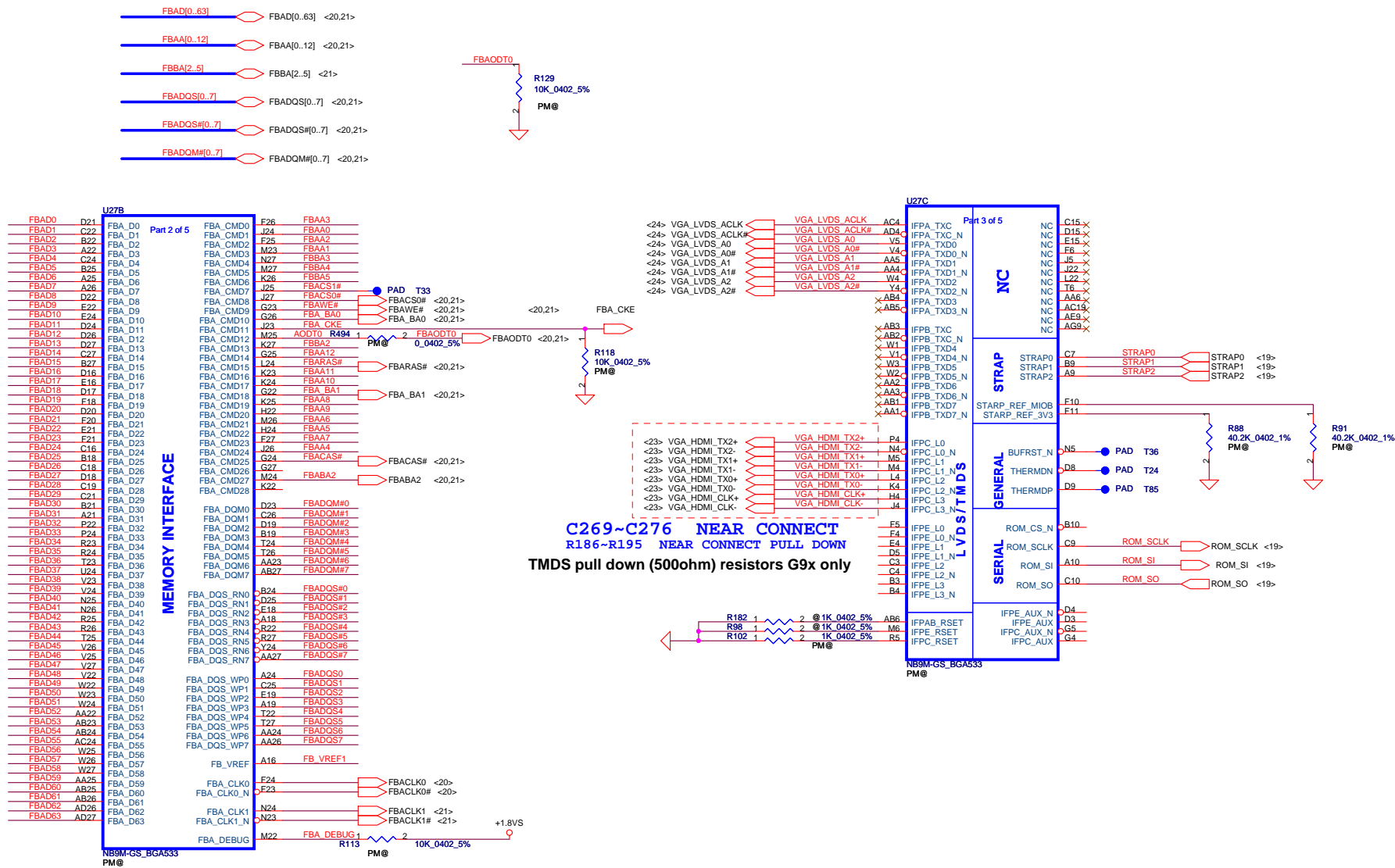


same with intel DDR3 CRB connection

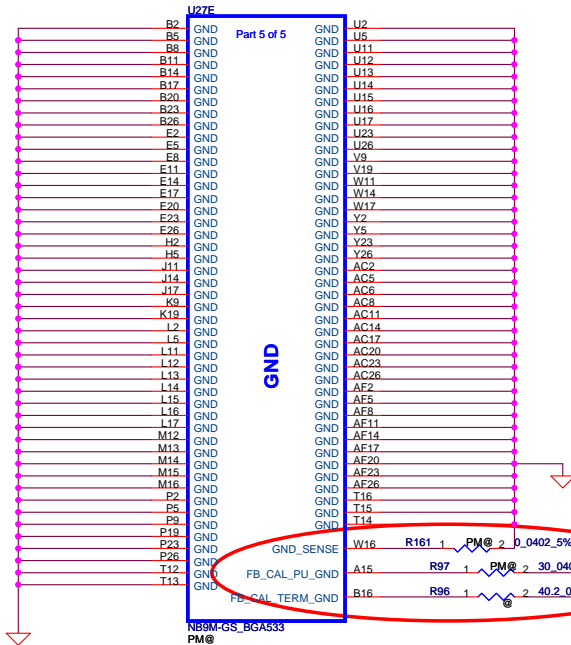
DDR3 SO-DIMM B  
REVERSE

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				Size	Document Number
				Montevina UMA DDR3	
				Date	Friday, May 02, 2008
				Sheet	15 of 52

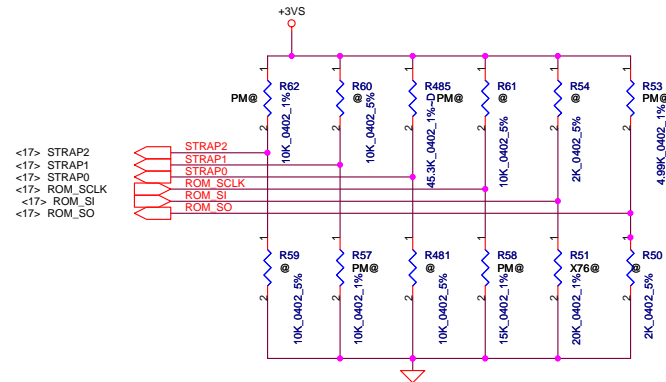








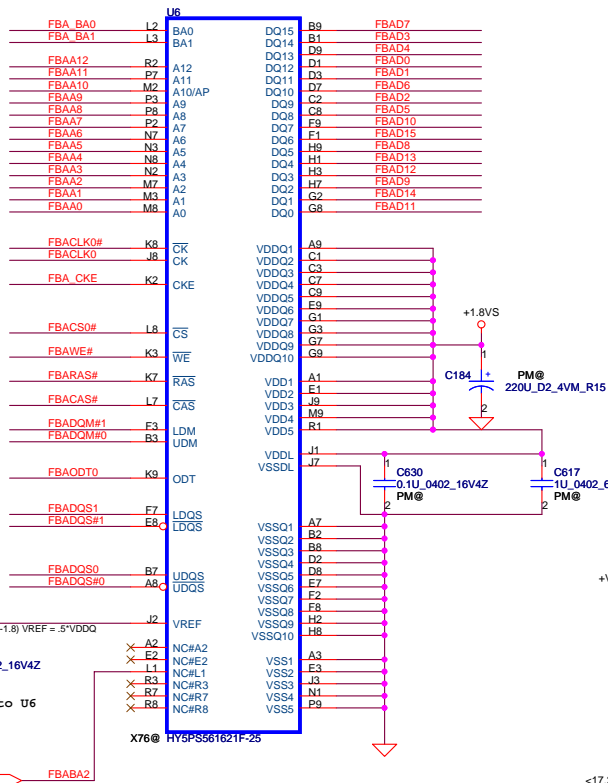
A total of 8 signals are required for GB1 strapping this includes  
 2 reference signals  
 6 physical strapping pins  
 4 logical strapping bits  
 A total of 24 logical strapping bits are available



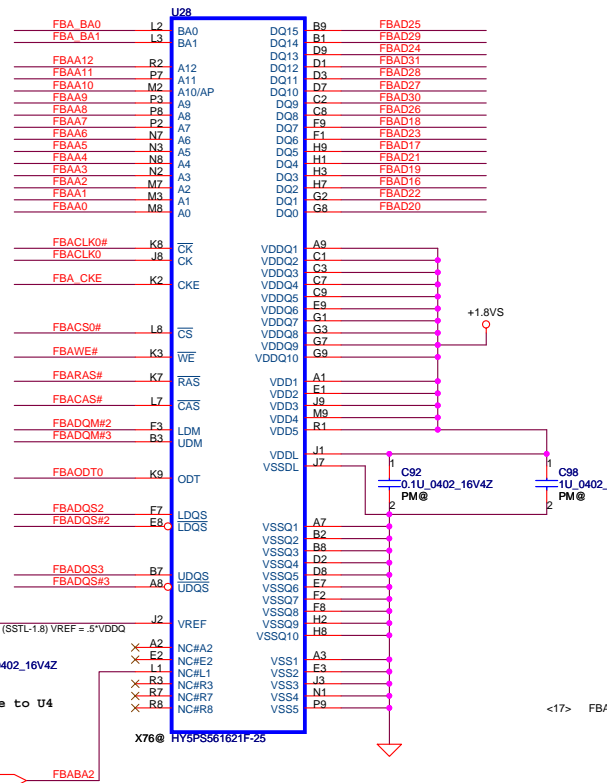
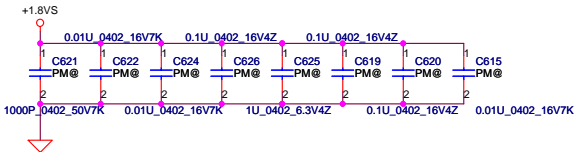
### GB1 Family GPU Strap Options

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K

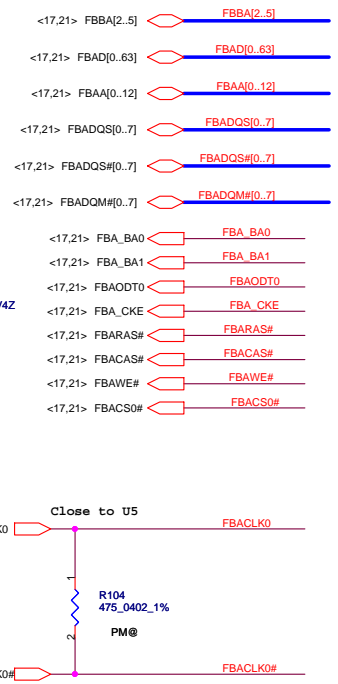
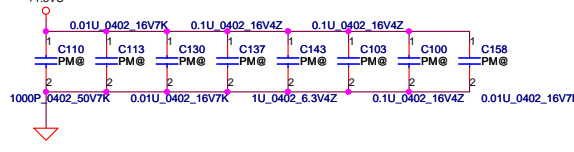
Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (32M*16)	Hynix	SA000012G30	X7611338L04
	Qimonda	SA00001YF10	X7611338L05
	Samsung	SA00001KH10	X7611338L06



DDR2 BGA MEMORY



DDR2 BGA MEMORY



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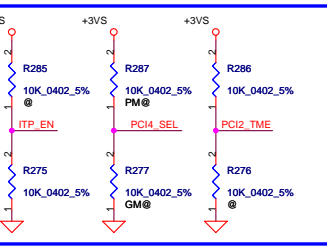
VRAM DDRA

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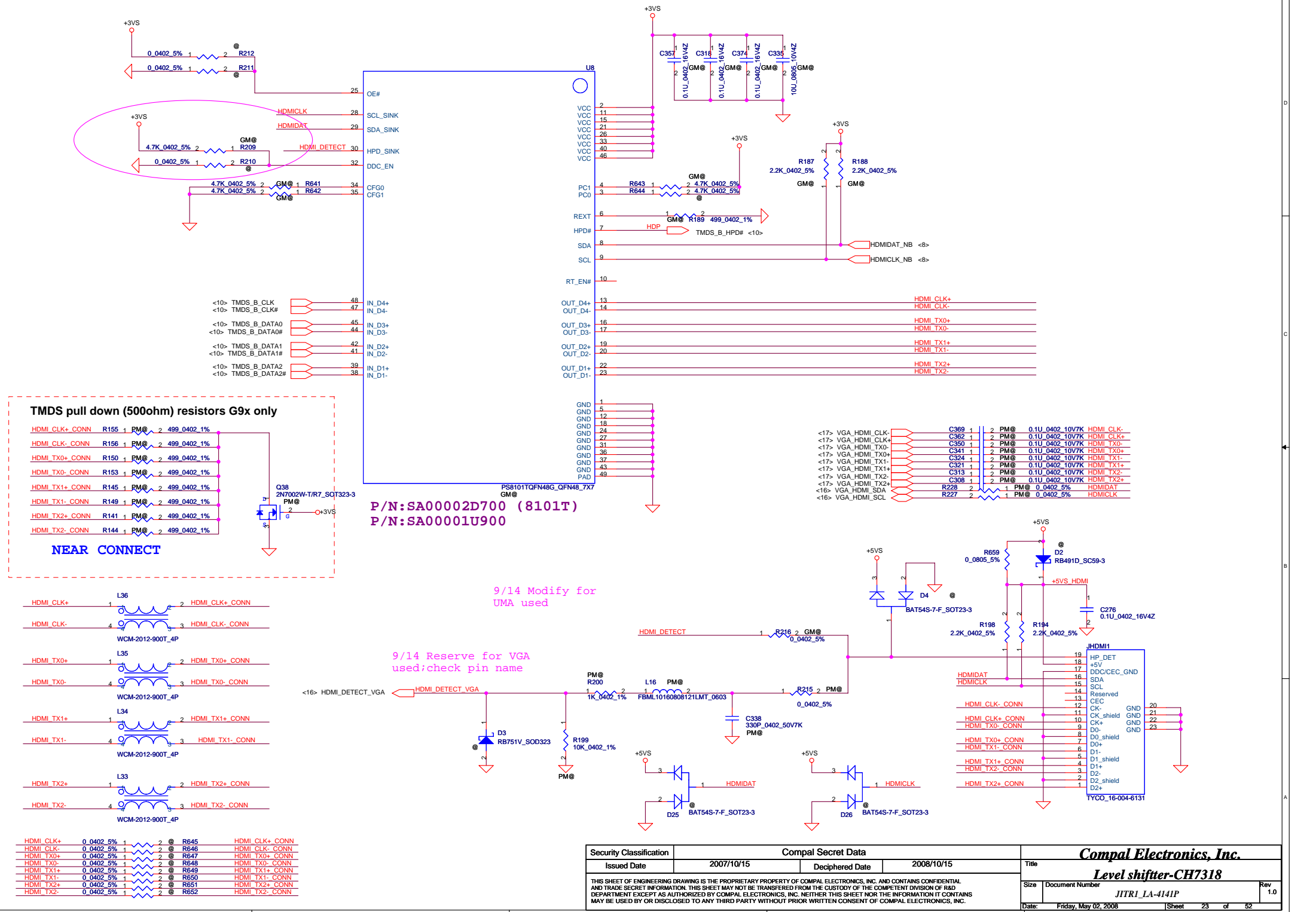
PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

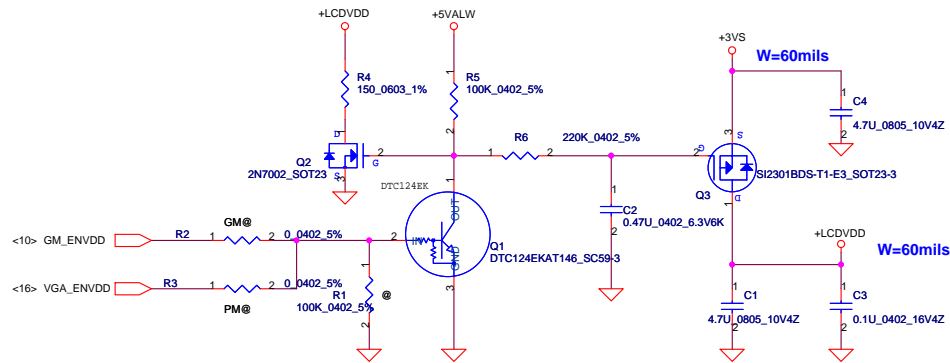
### **Clock generator**

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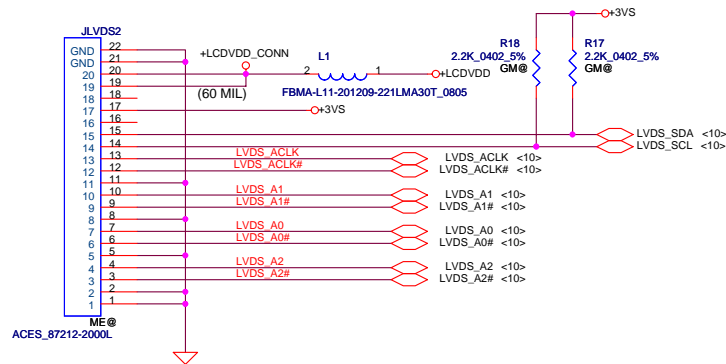


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<div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div>					<b>Level shifter-CH7318</b>		
					Size	Document Number	Rev
						JITRI_LA-4141P	1.0
					Date:	Friday, May 02, 2008	Sheet 23 of 52

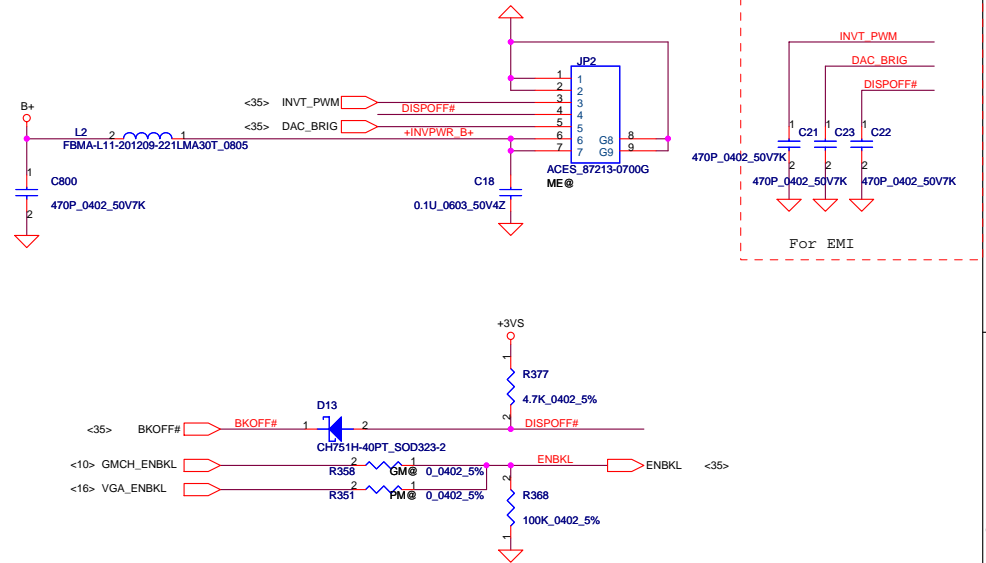
## LCD POWER CIRCUIT



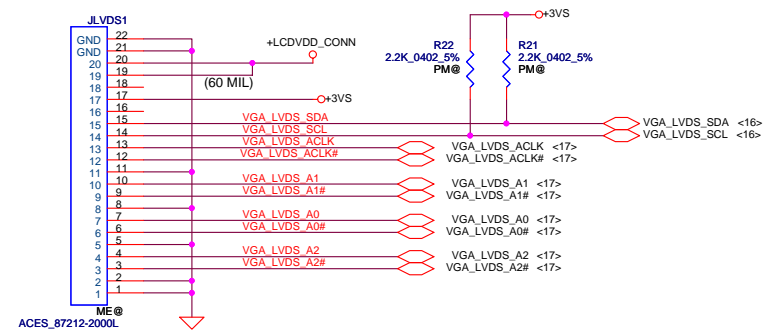
## LCD/PANEL BD. Conn.



## INVERTER Conn.



## LCD/PANEL BD. Conn.



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					Size B	Document Number	Rev
						JITR1_LA-4141P	0.1
					Date:	Friday, May 02, 2008	Sheet 24 of 52

Compal Electronics, Inc.

LVDS & DVI Connector

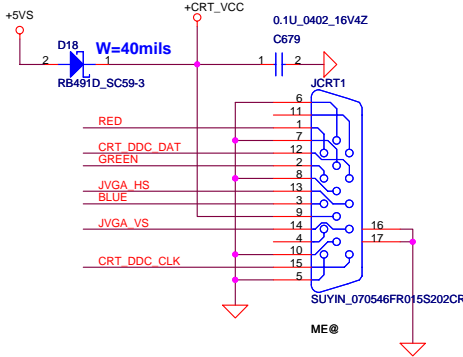
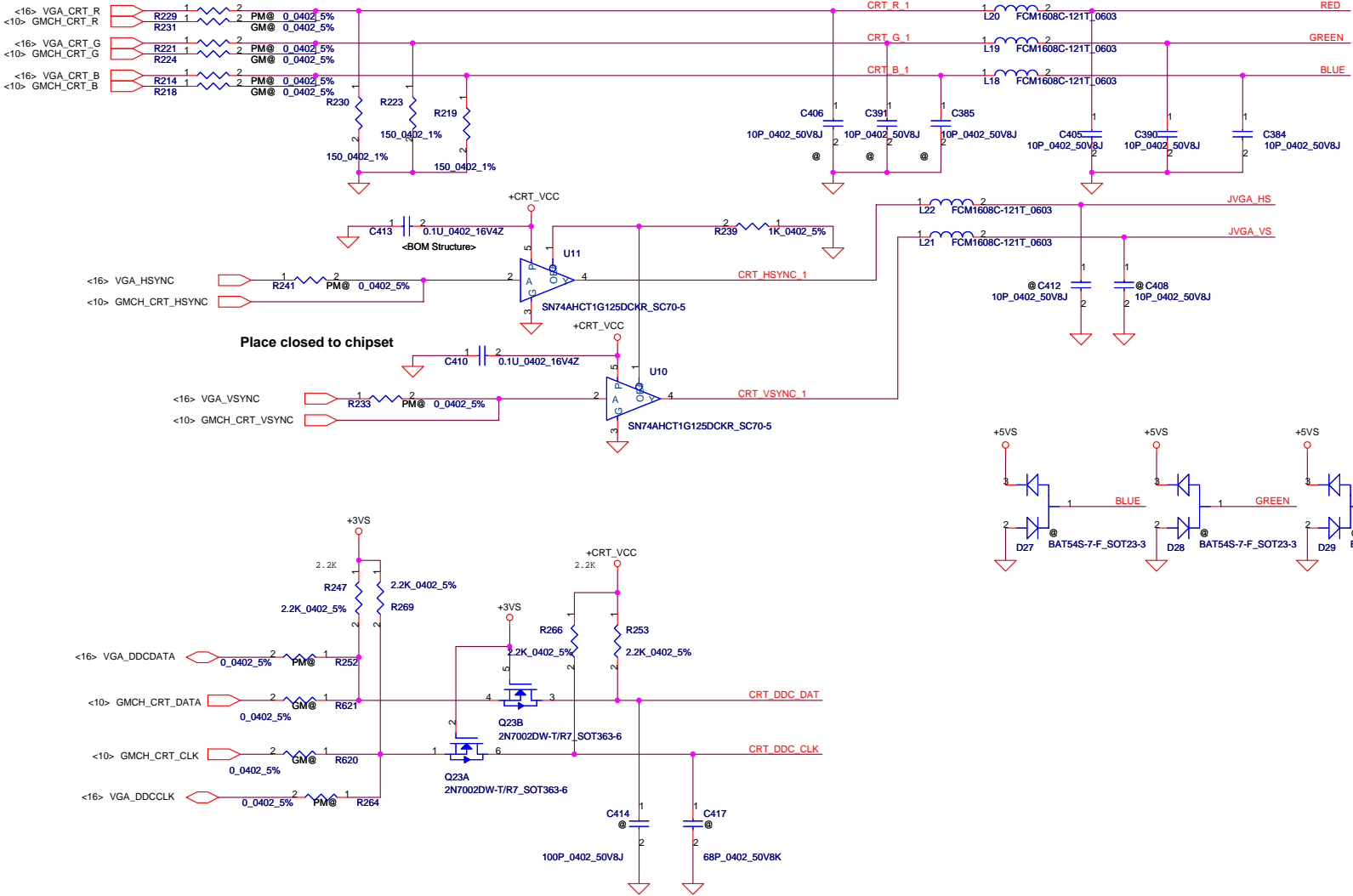
JITRI\_LA-4141P

Rev

0.1

CRT Connector

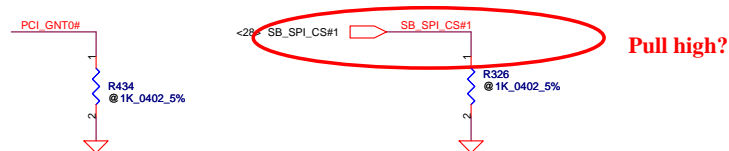
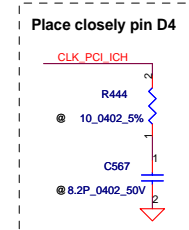
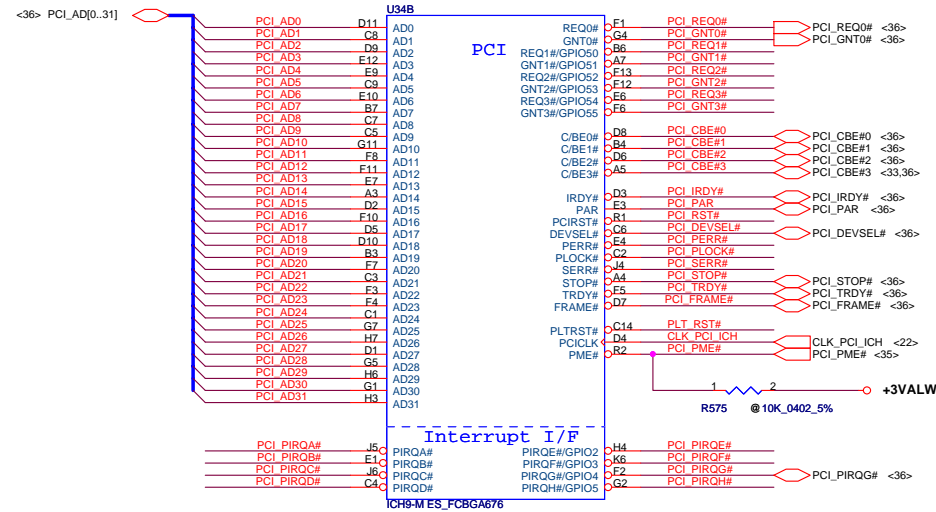
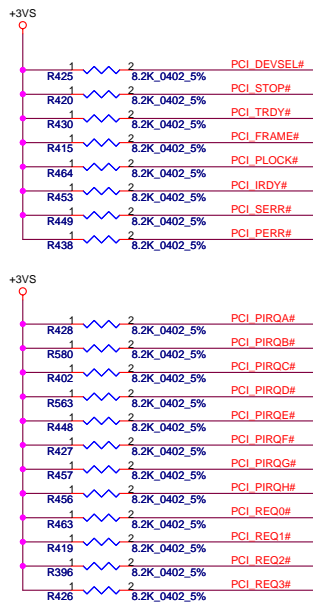
Place closed to chipset



PIN ASSIGMENT

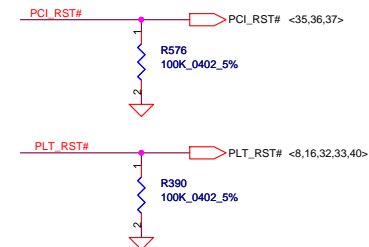
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VS
10	GND
13	HS
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

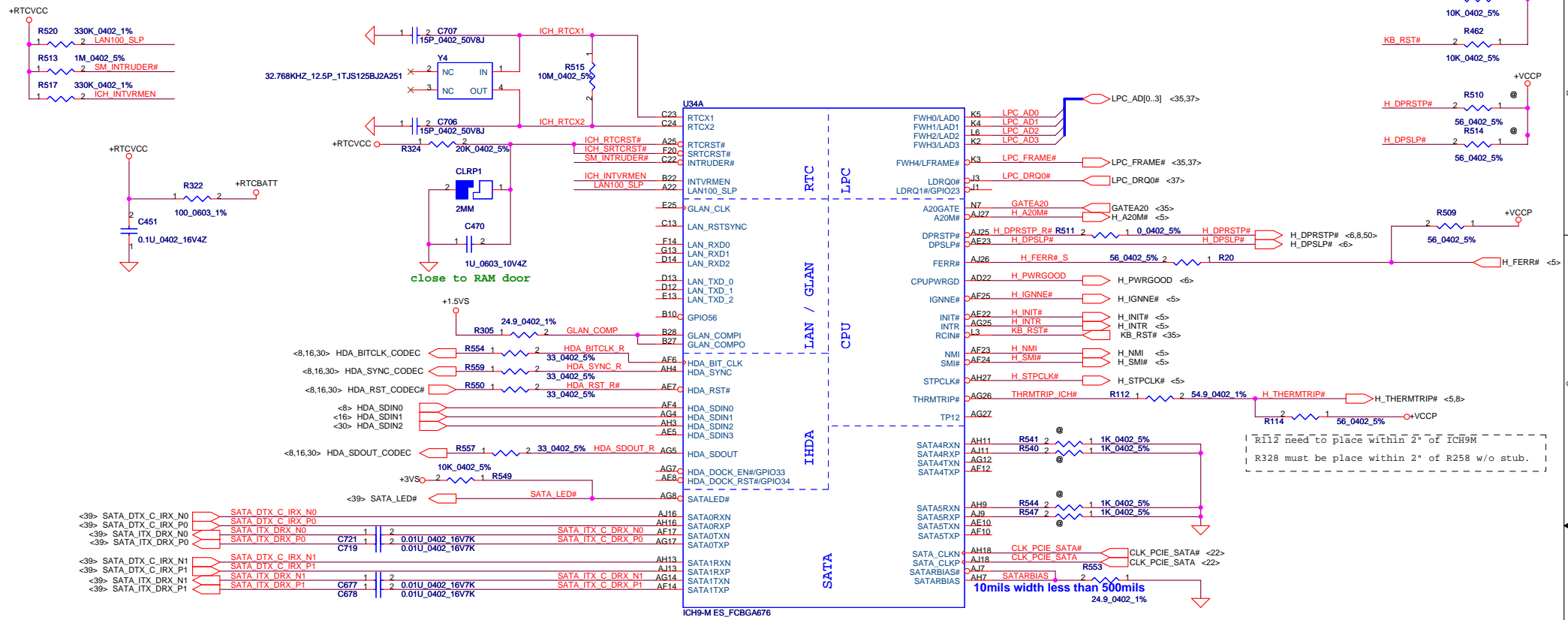
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Size	Document Number	JITR1_LA-4141P		Rev
Custom				0.1
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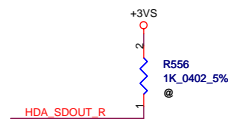
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*





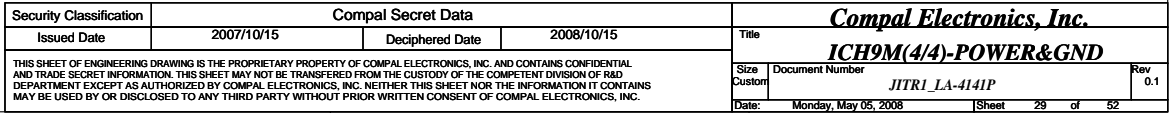
Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1



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				Custom	<b>JITRI_LA-414IP</b>	
				Date:	Friday, May 02, 2008	Sheet 28 of 52



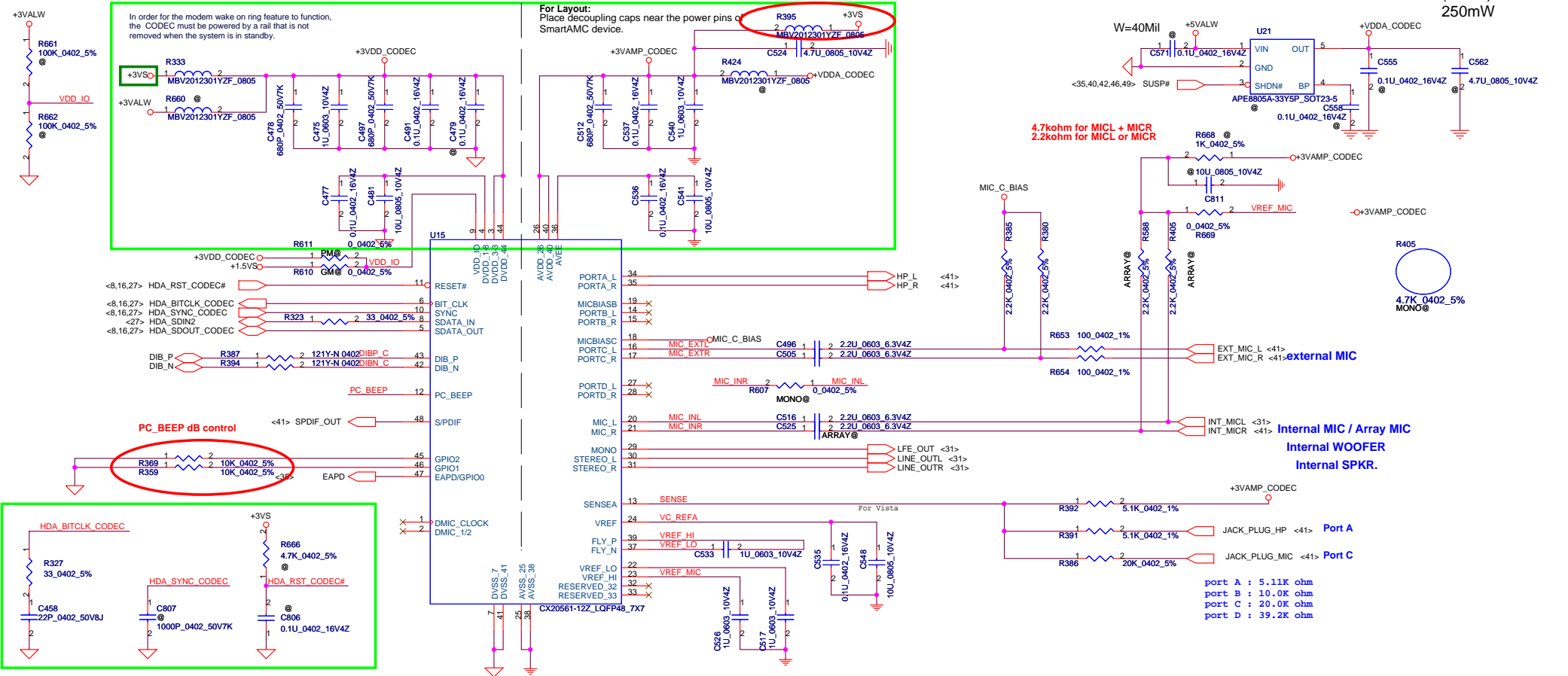
# AUDIO CODEC

0308\_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680pF

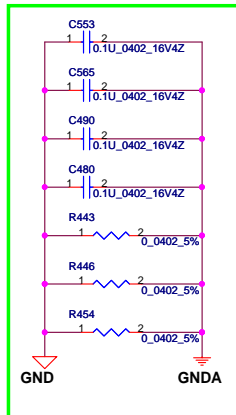
CHANGE TO 0ohm (2008/05/05)

# CODEC POWER

(3.33V)  
250mW



## DIGITAL ANALOG

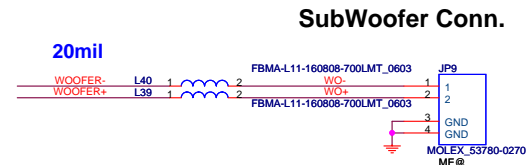


Place these C and R around AGND and DGND,  
then choose the one which is close to Codec

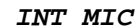
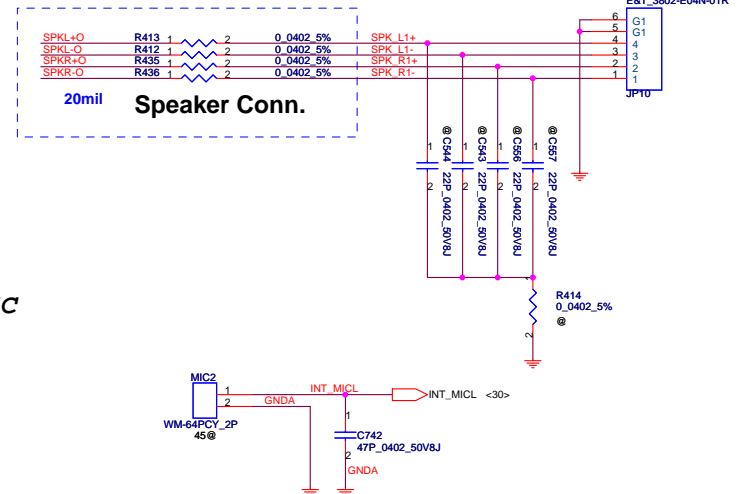
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1st = APA3011 (SA00001JM00)  
2nd = TPA6211 (SA621110010 )



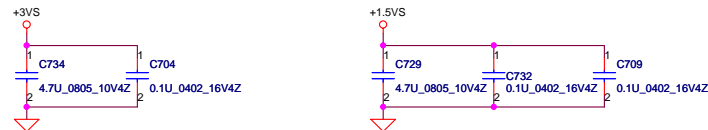
1st = APA2031 (SA00001RZ00)  
2nd = G1431F2U (SA000012Y00)



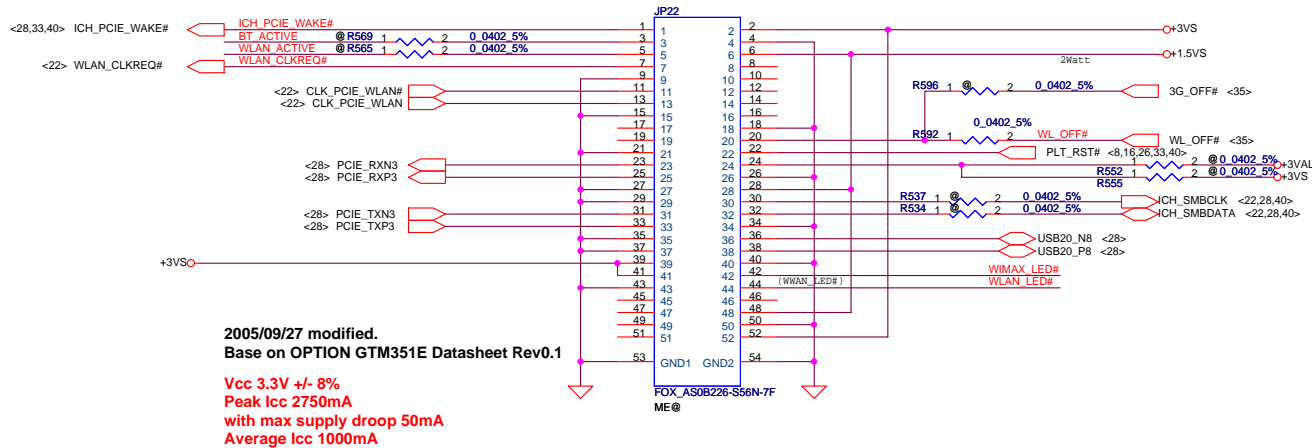
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>AMP/VR/Audio Jack/MIC</b>			
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				Custom	JITRI_LA-414IP	0.1	
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# Mini-Express Card for 3G Or TV Tuner

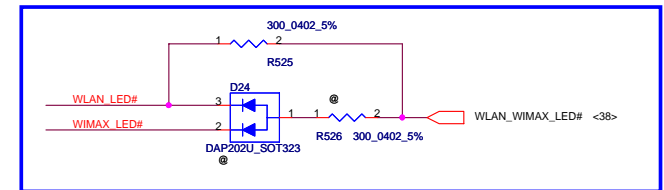
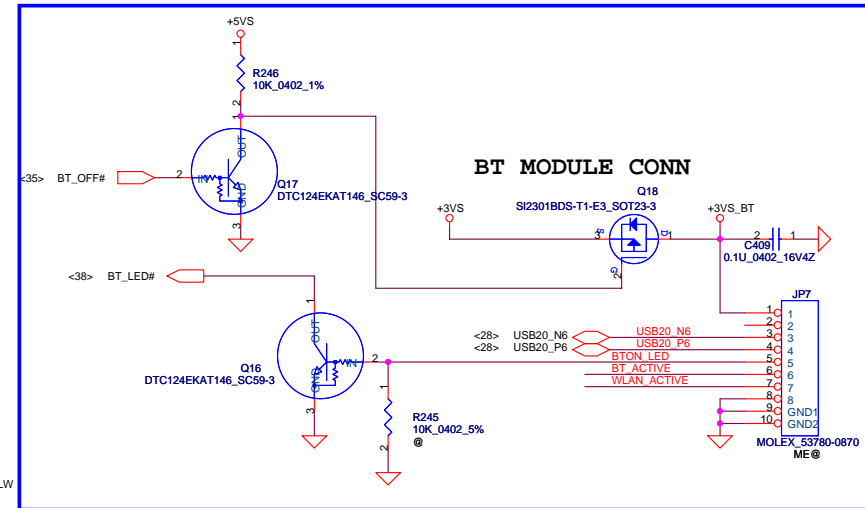
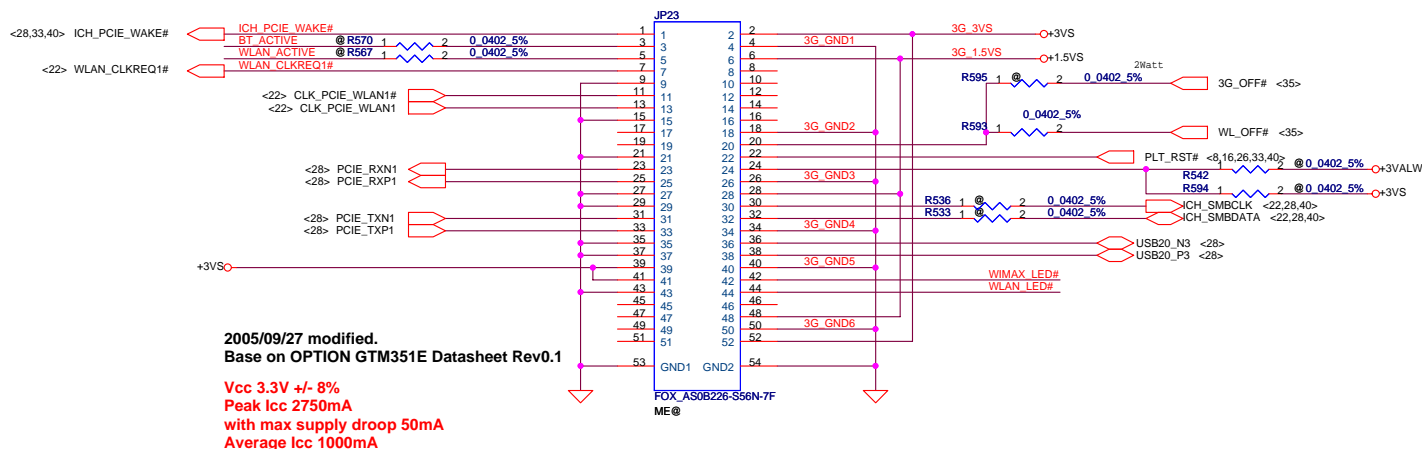
## Mini-Express Card for WLAN



### Mini-Express Card(Slot 1-WLAN WIMAX)

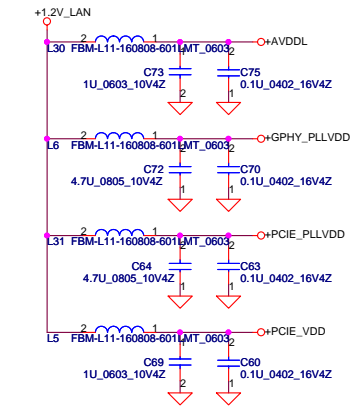
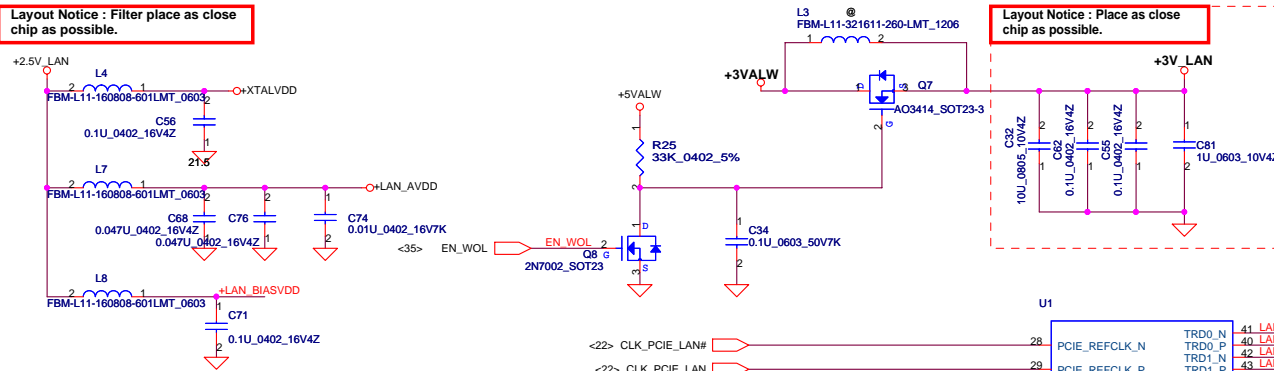


### Mini-Express Card(Slot 2-WLAN WIMAX)

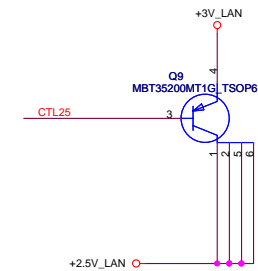
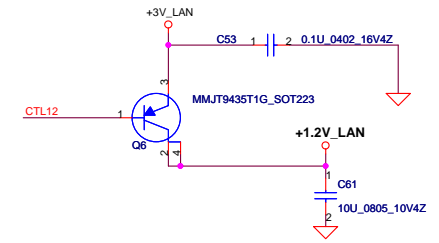
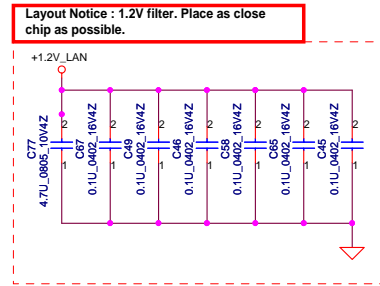
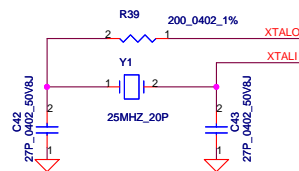
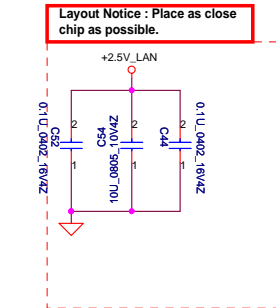
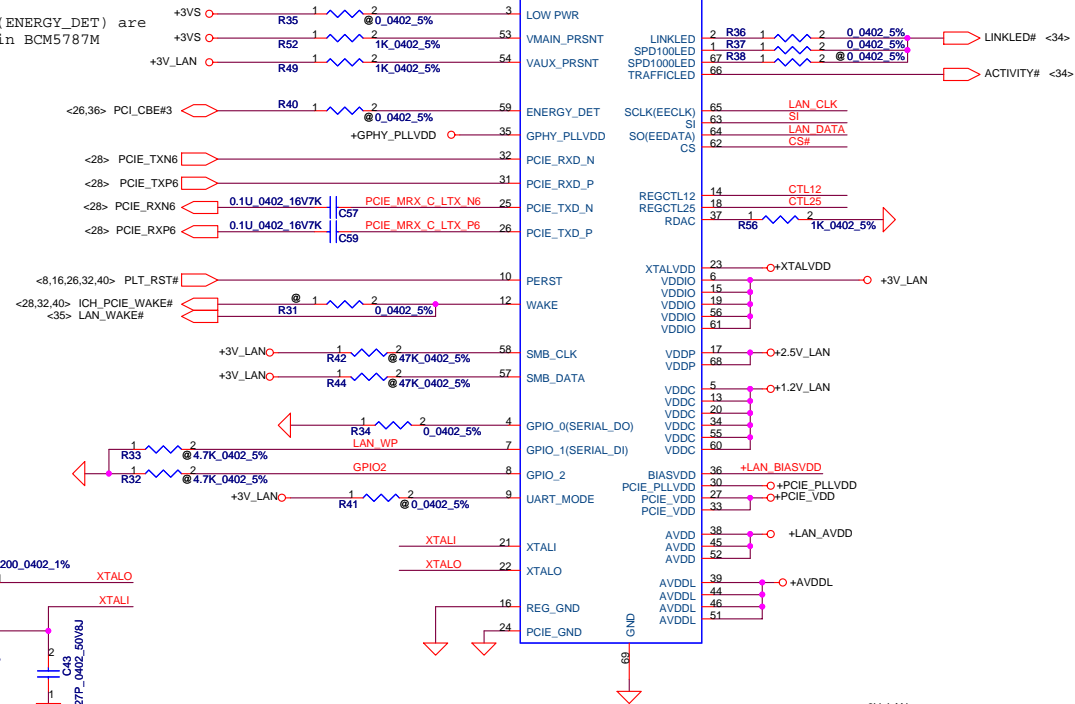


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Size		Document Number		Rev	
Date		Monday, May 05, 2008		Sheet 32 of 52	
				JITRI_LA-4141P	
				0.1	

**Layout Notice : Filter place as close chip as possible.**

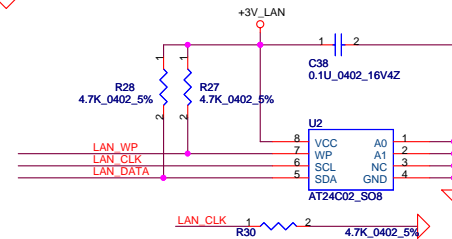


(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M

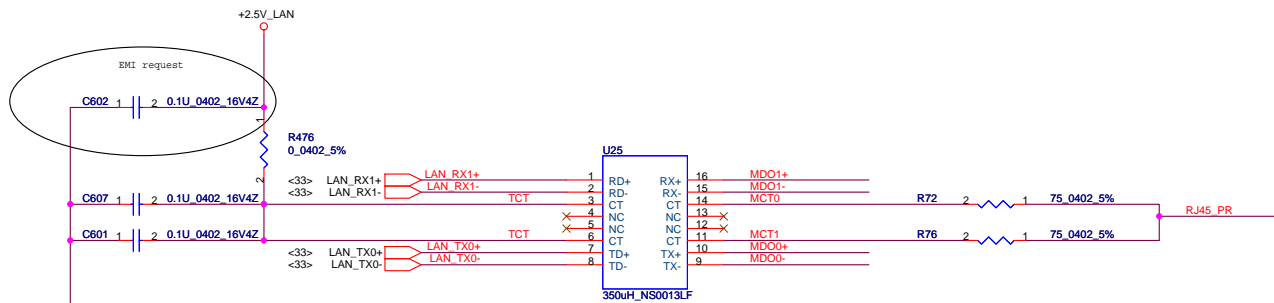


Notice : 4.7u 6.3V capactor Thickness 1.25mm

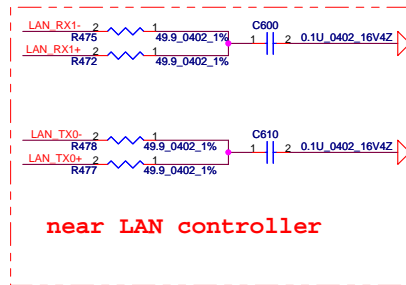
**Layout Notice : Filter place as close chip as possible.**



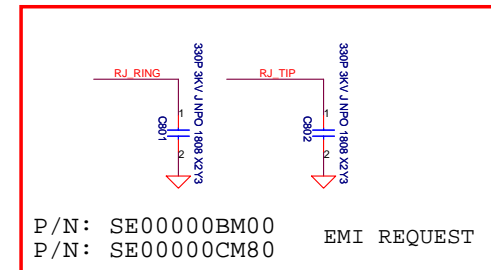
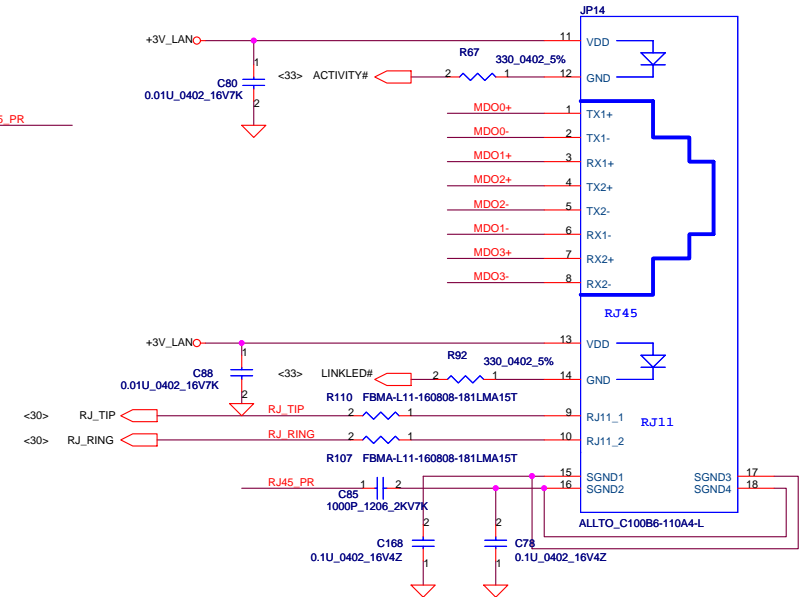
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title <b>BCM5787MKML</b>		
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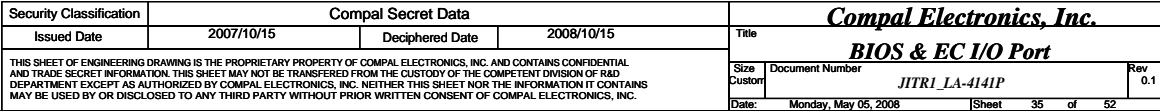
Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

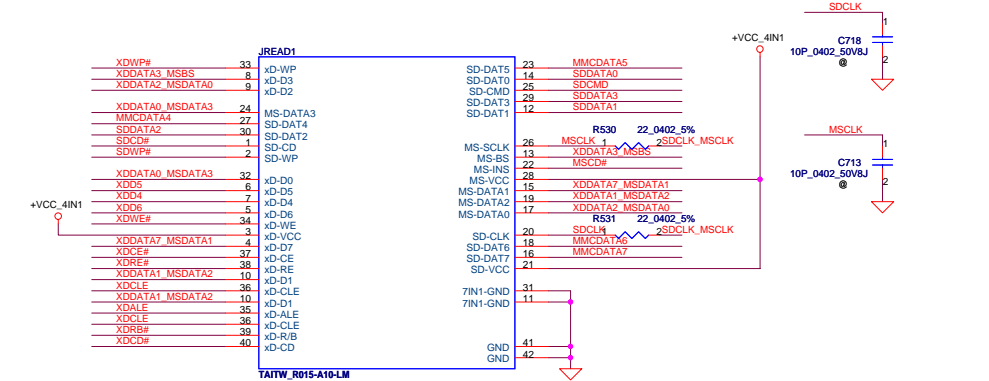
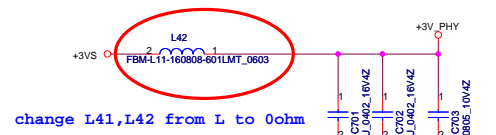
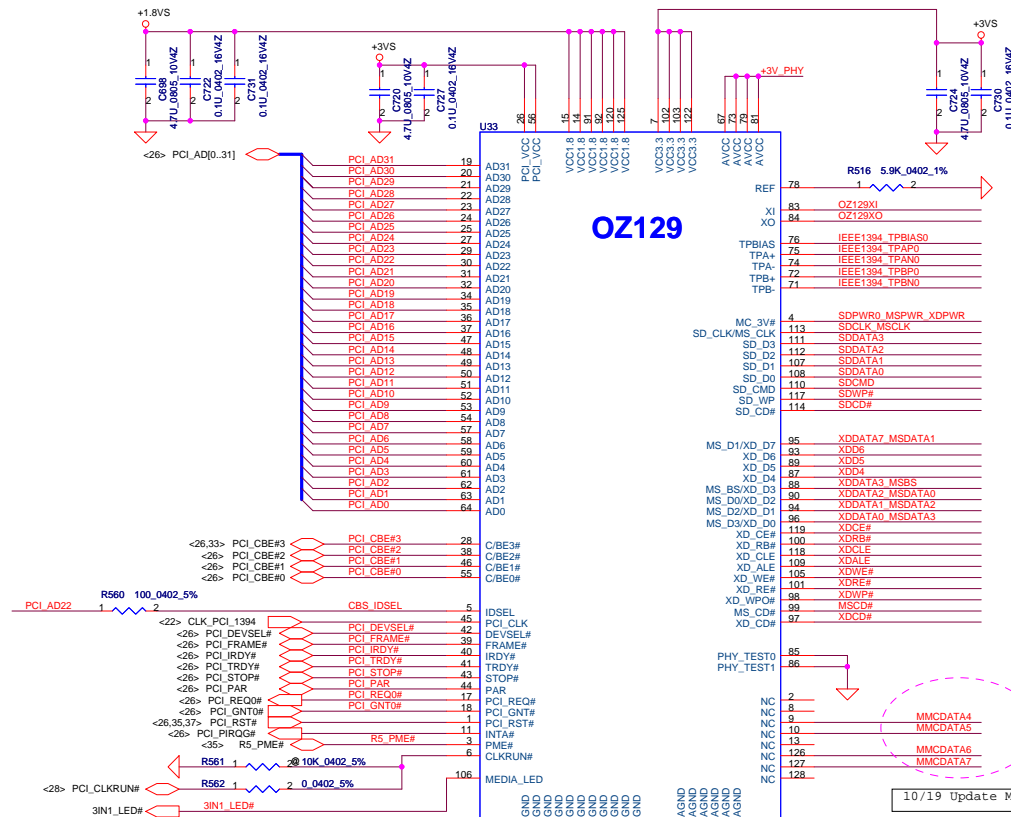


## RJ11+RJ45 CONN

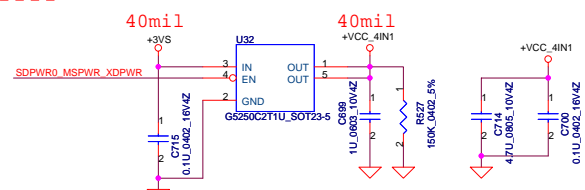
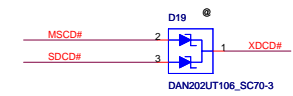
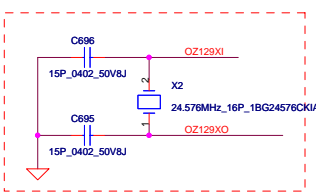
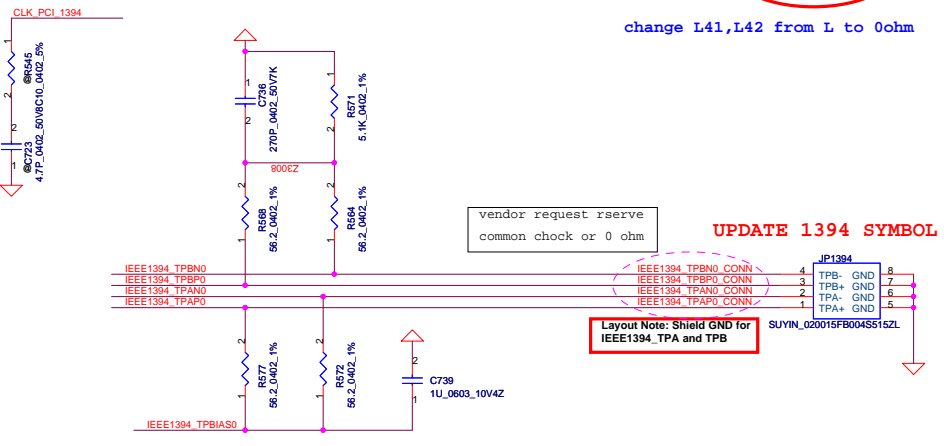


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				Rev	0.1





LED behave:  
Idel -----> low  
Access data --> always high

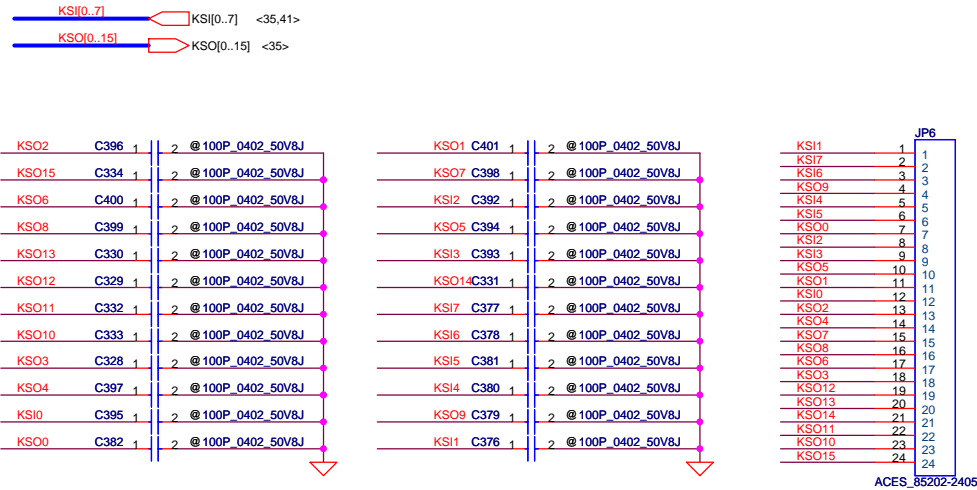


UPDATE 1394 SYMBOL

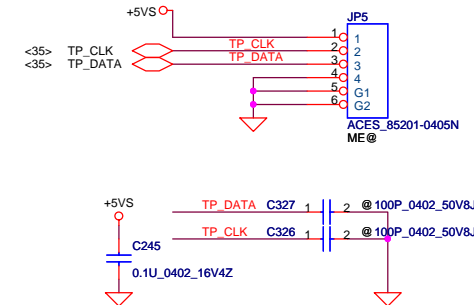
Layout Note: Shield GND for IEEE1394\_TPA and TPB

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Title		Compal Electronics, Inc.	
1394+3 in 1 Card		Rev 0.1	
Date		Friday, May 02, 2008	
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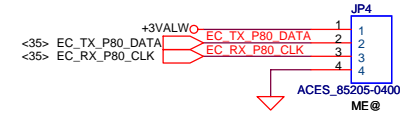
## INT\_KBD Conn.



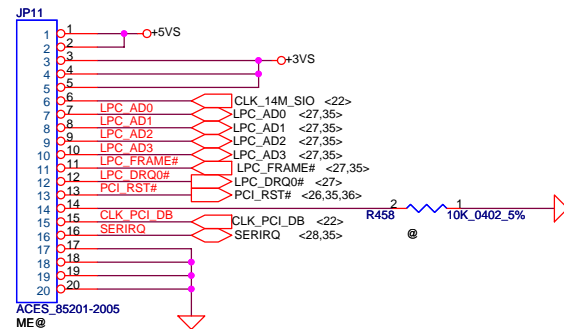
## To TP/B Conn.



## EC DEBUG PORT

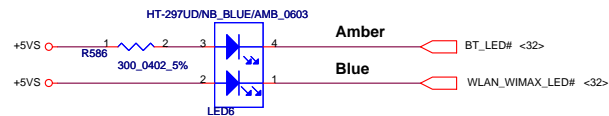
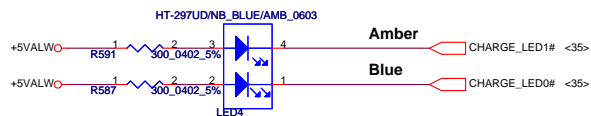
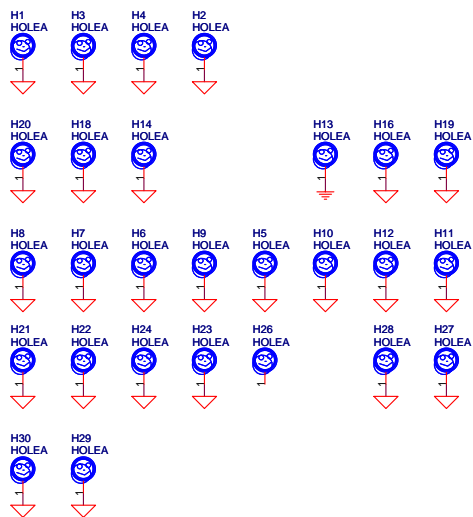
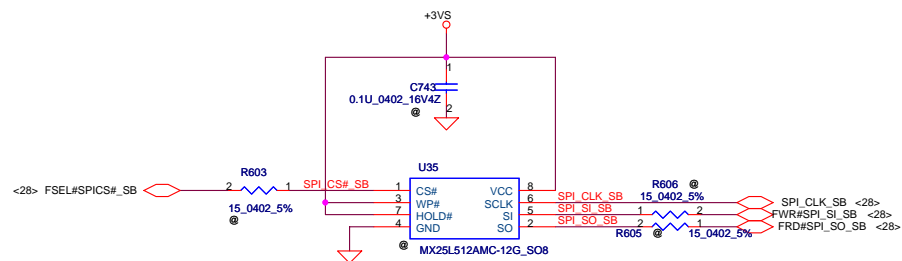


## FOR LPC SIO DEBUG PORT

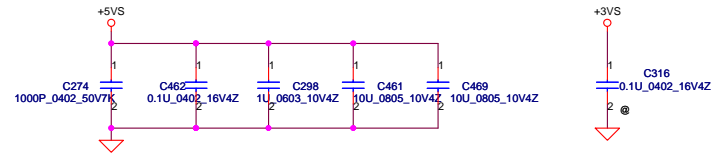


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				JITR1_LA-4141P	
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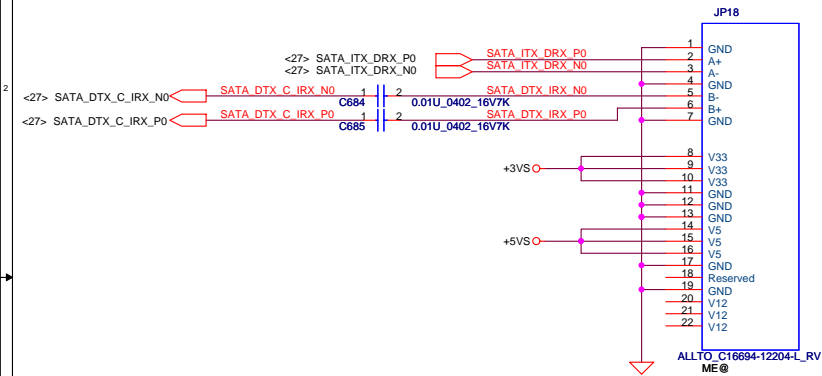
## +3VALW



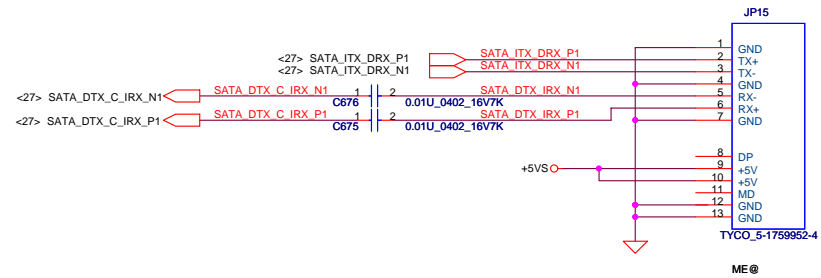
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>LED/EC SPI ROM</b>	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				B	0
				Document Number JI7RI_LA-4141P	
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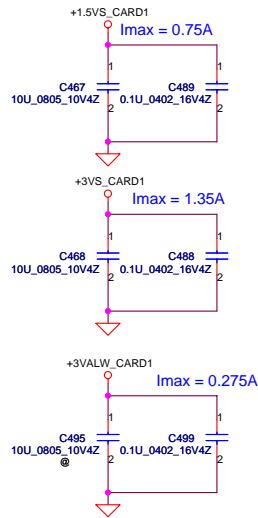
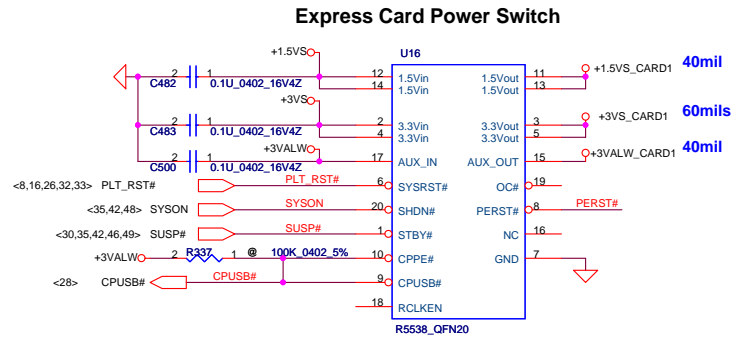
### SATA HDD Conn.



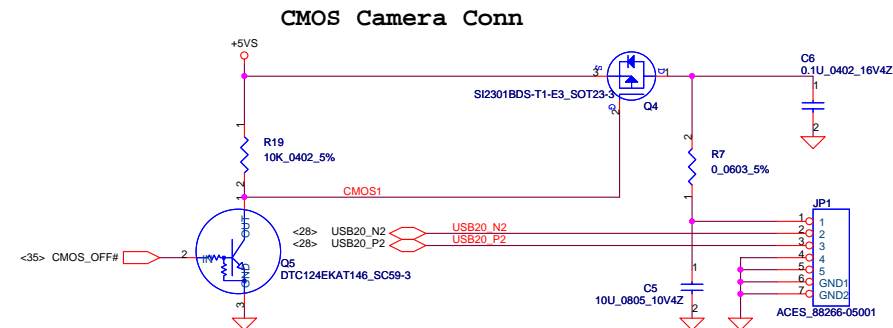
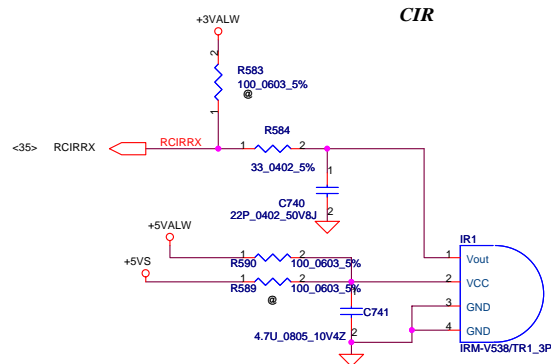
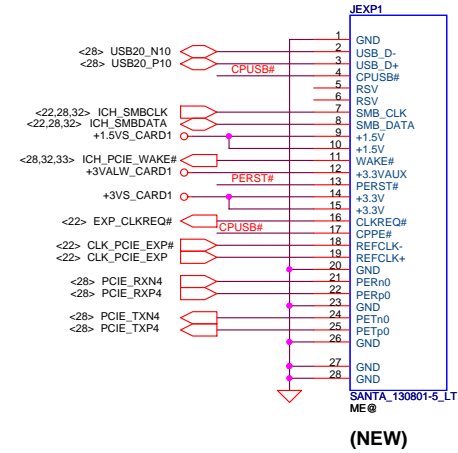
### SATA ODD Conn.



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### New Card Socket (Left/TOP)

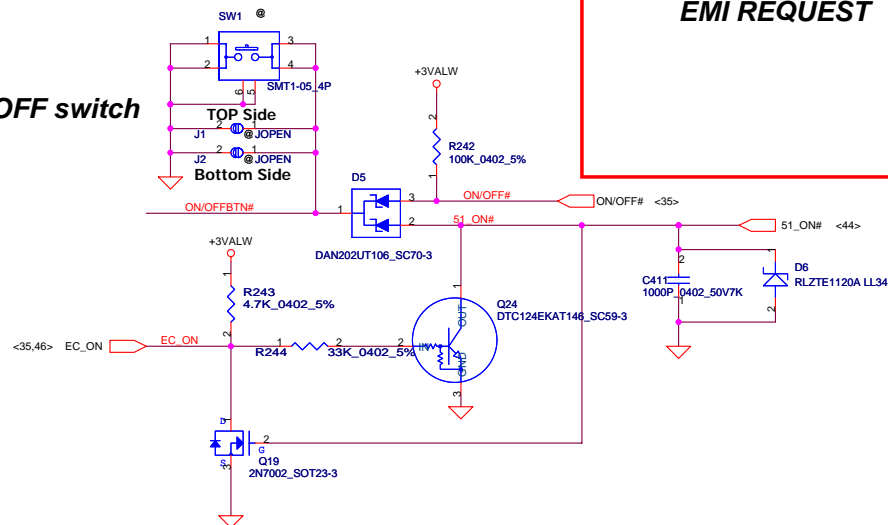


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Date: Friday, May 02, 2008				Rev	0.1

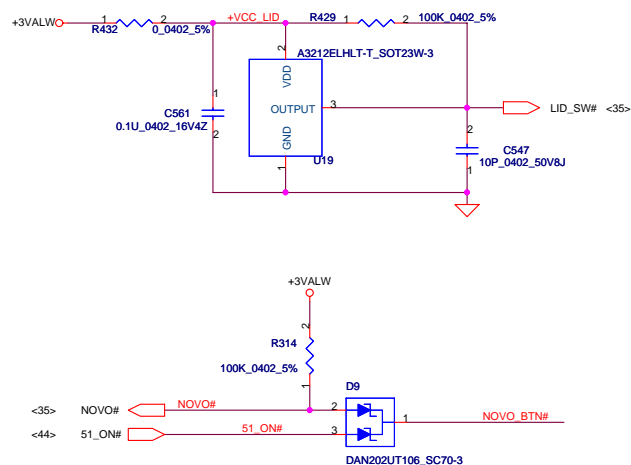
**Switch Board Conn.**



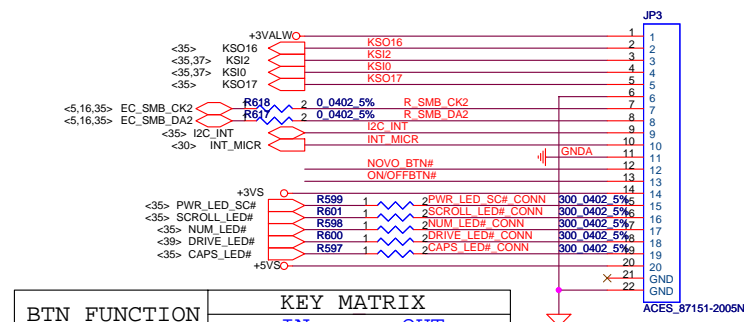
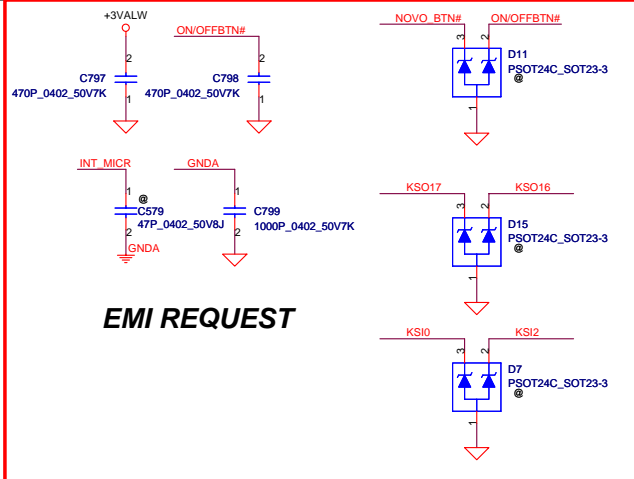
**ON/OFF switch**



### ***Lid Switch***

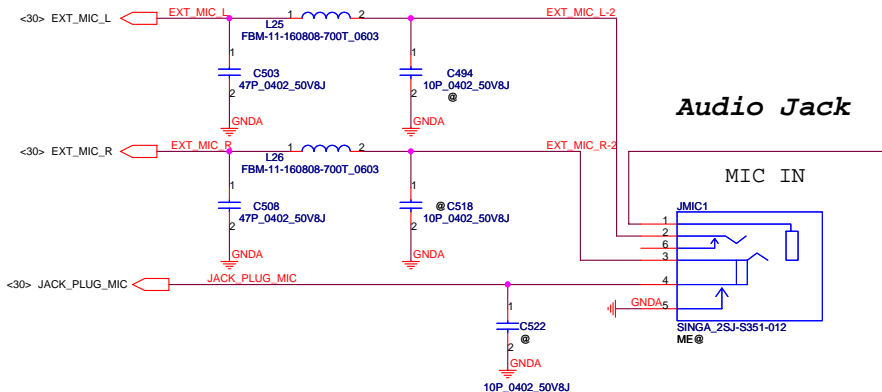


## EMI REQUEST

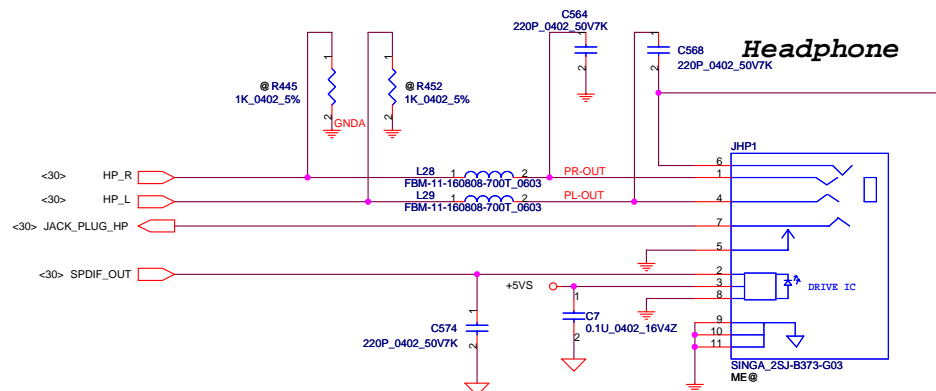


BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KS016	KS12
DOWN	KS017	KS12
OK	KS017	KS10

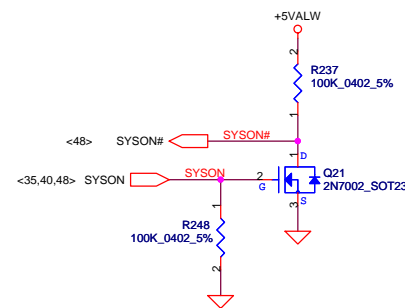
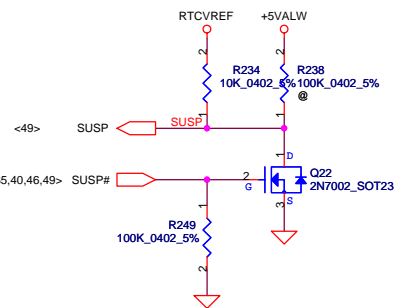
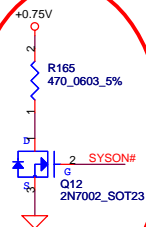
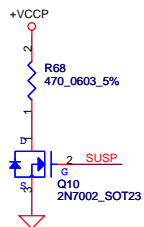
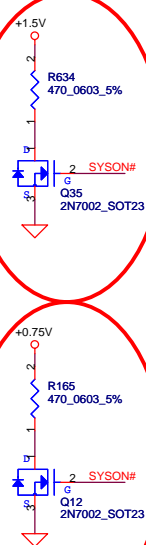
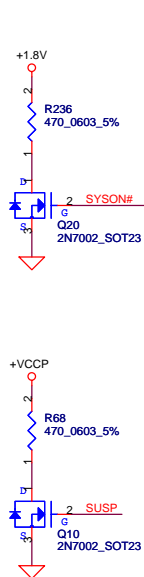
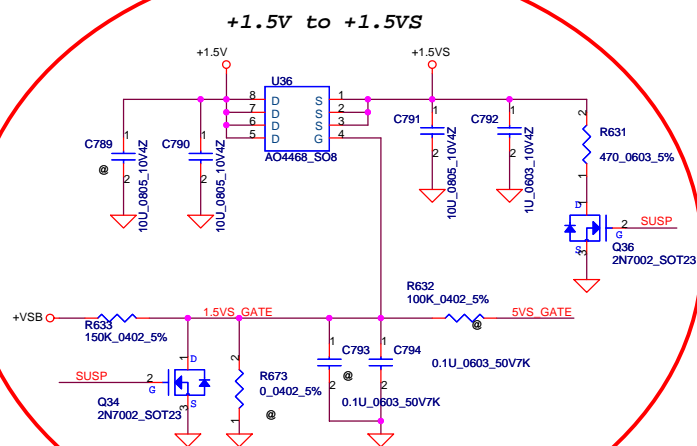
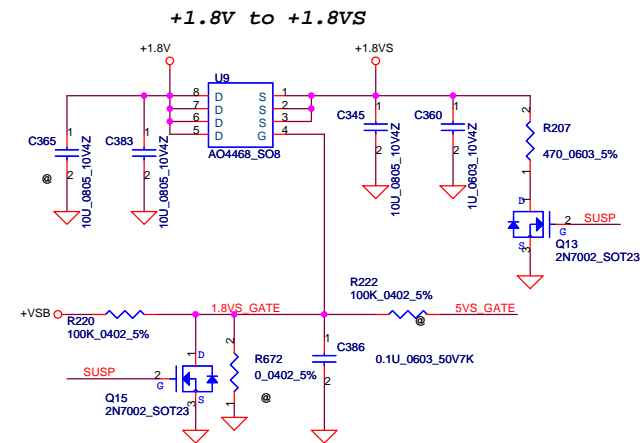
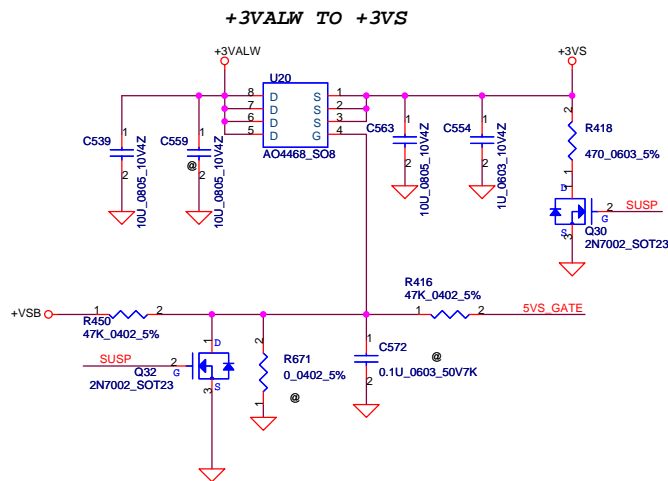
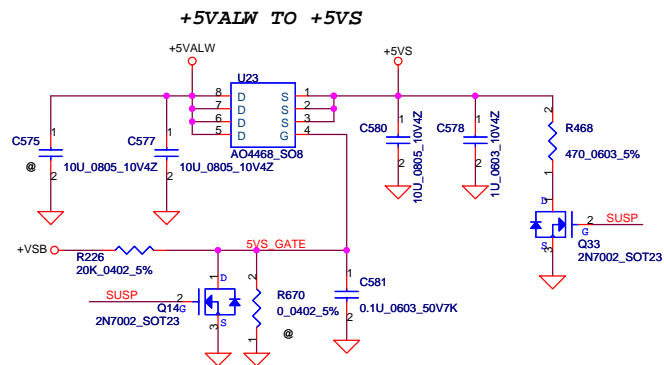
## Audio Jack



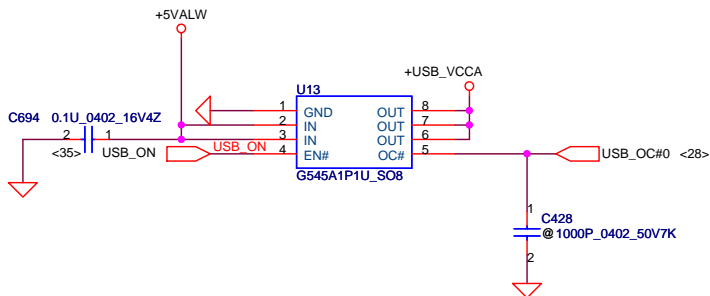
### Headphone



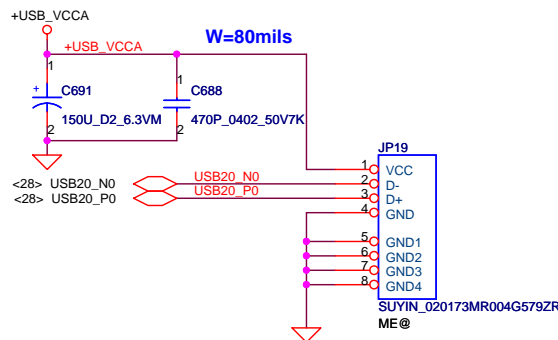
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								<b>Audio Jack &amp; SW connector</b>	
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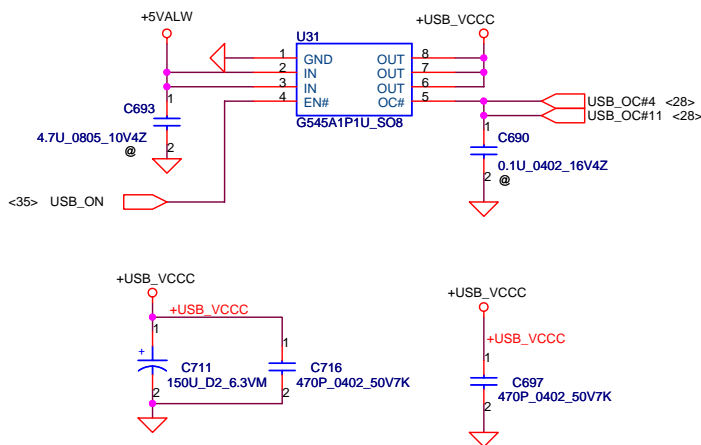
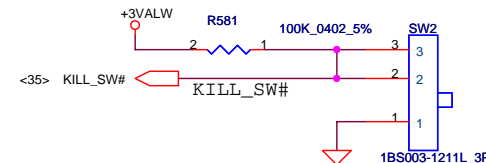
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		1.0	
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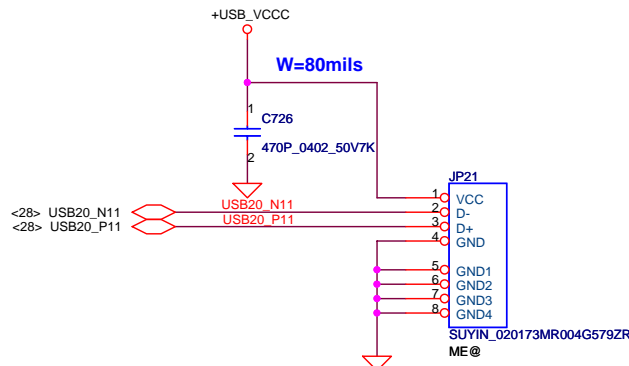
## LIFT USB CONN. 1



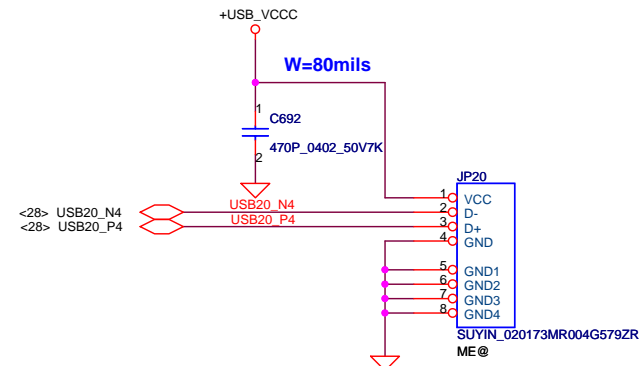
## Kill Switch



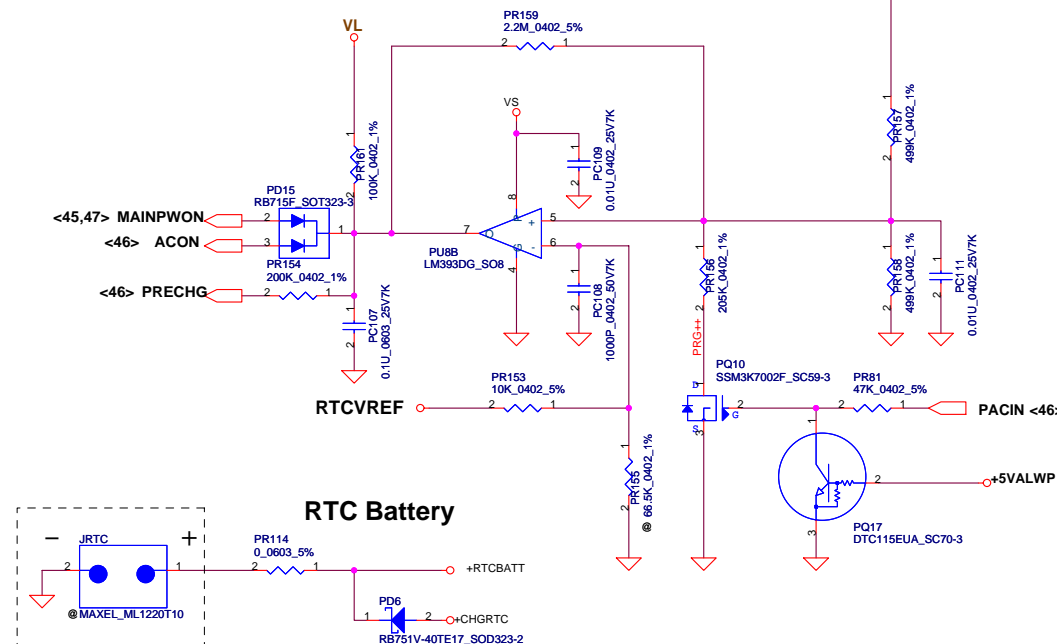
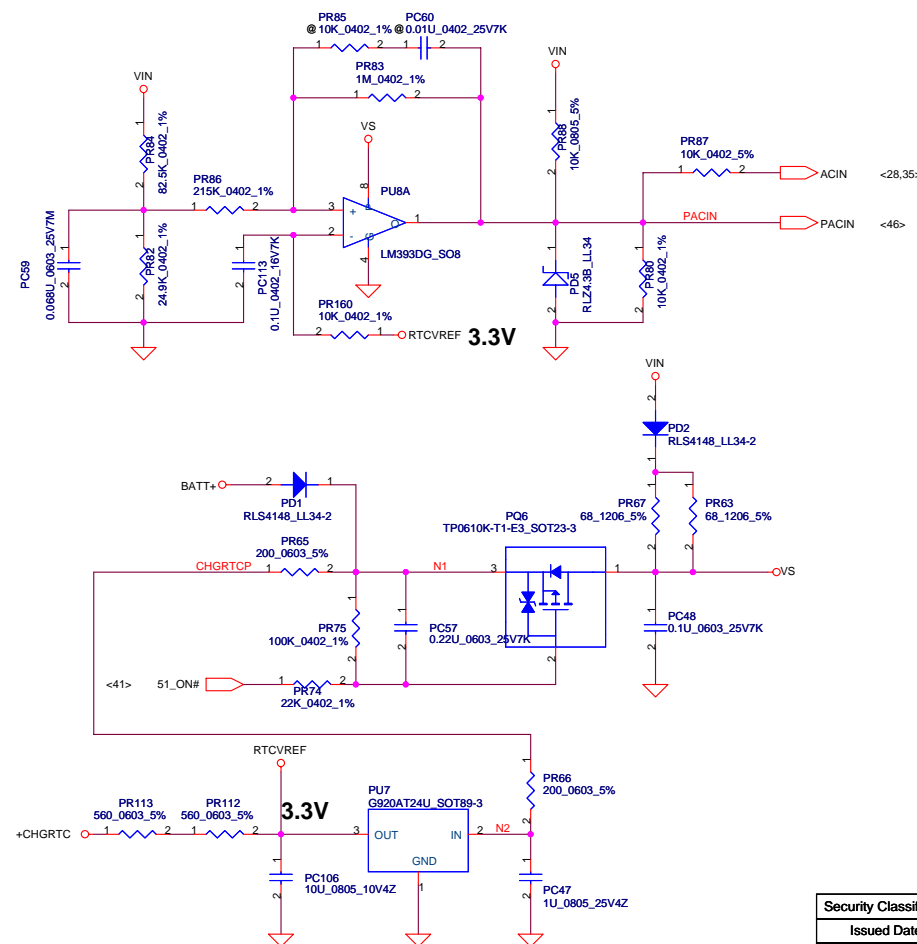
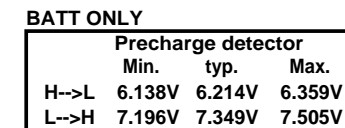
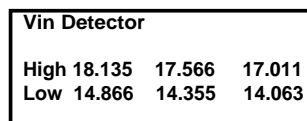
## RIGHT USB CONN. 3



## RIGHT USB CONN. 2

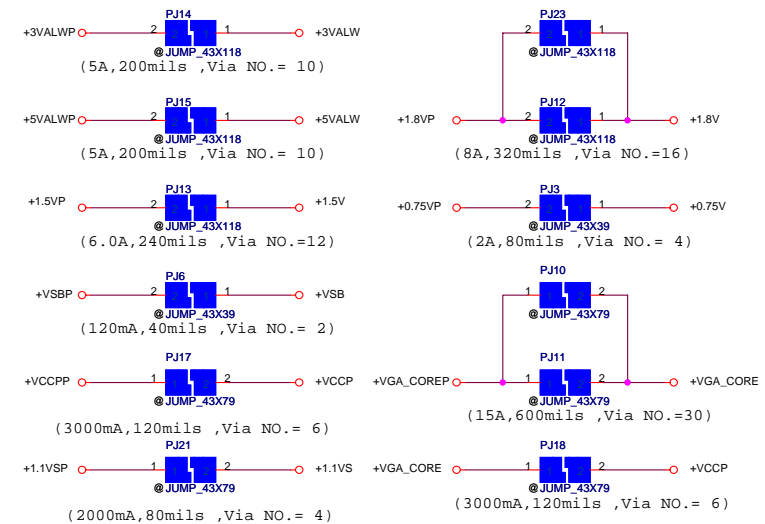
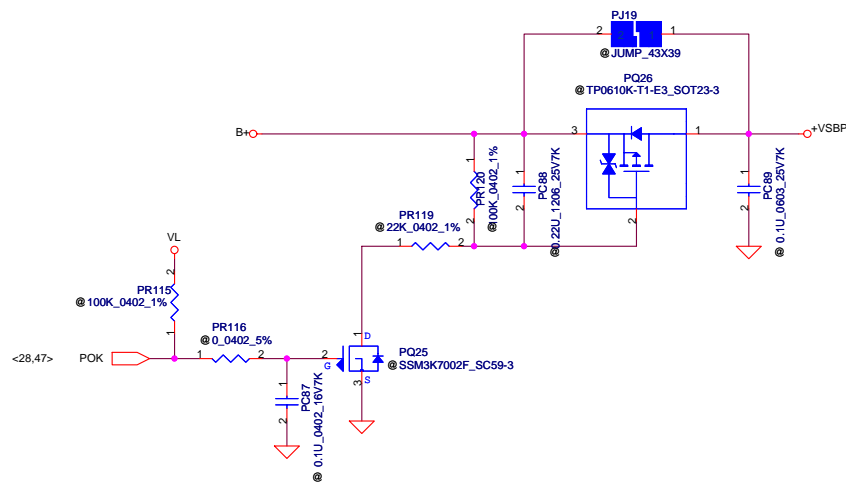
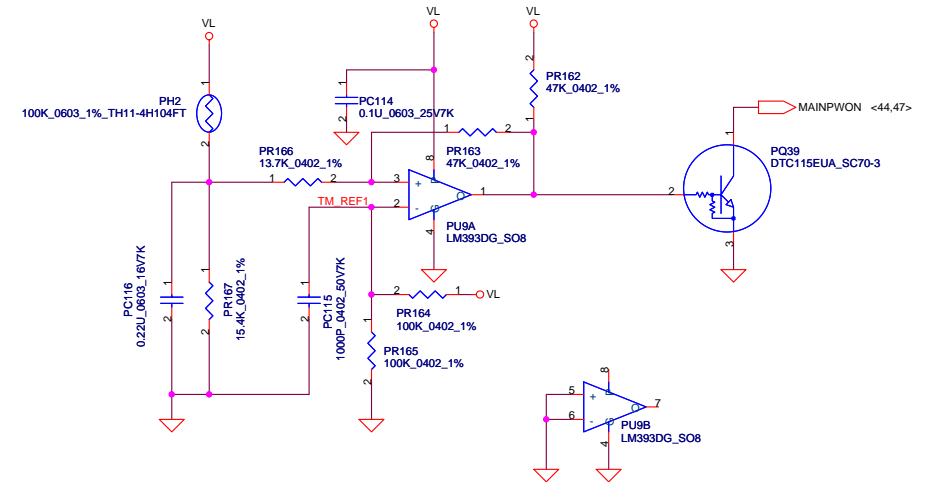
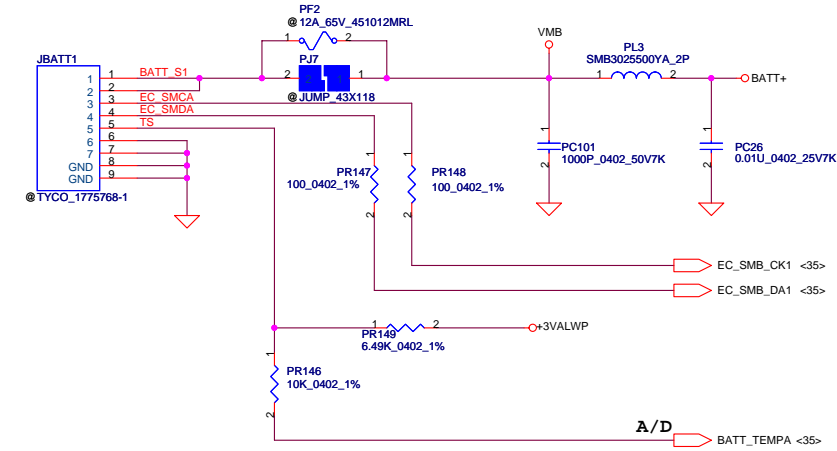


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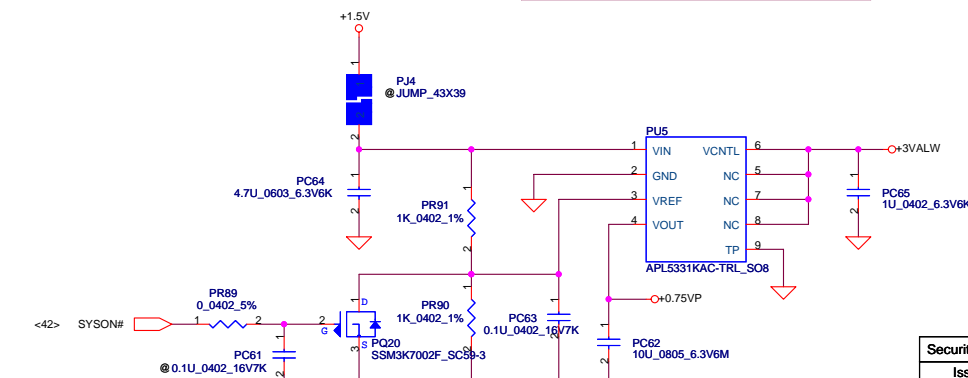
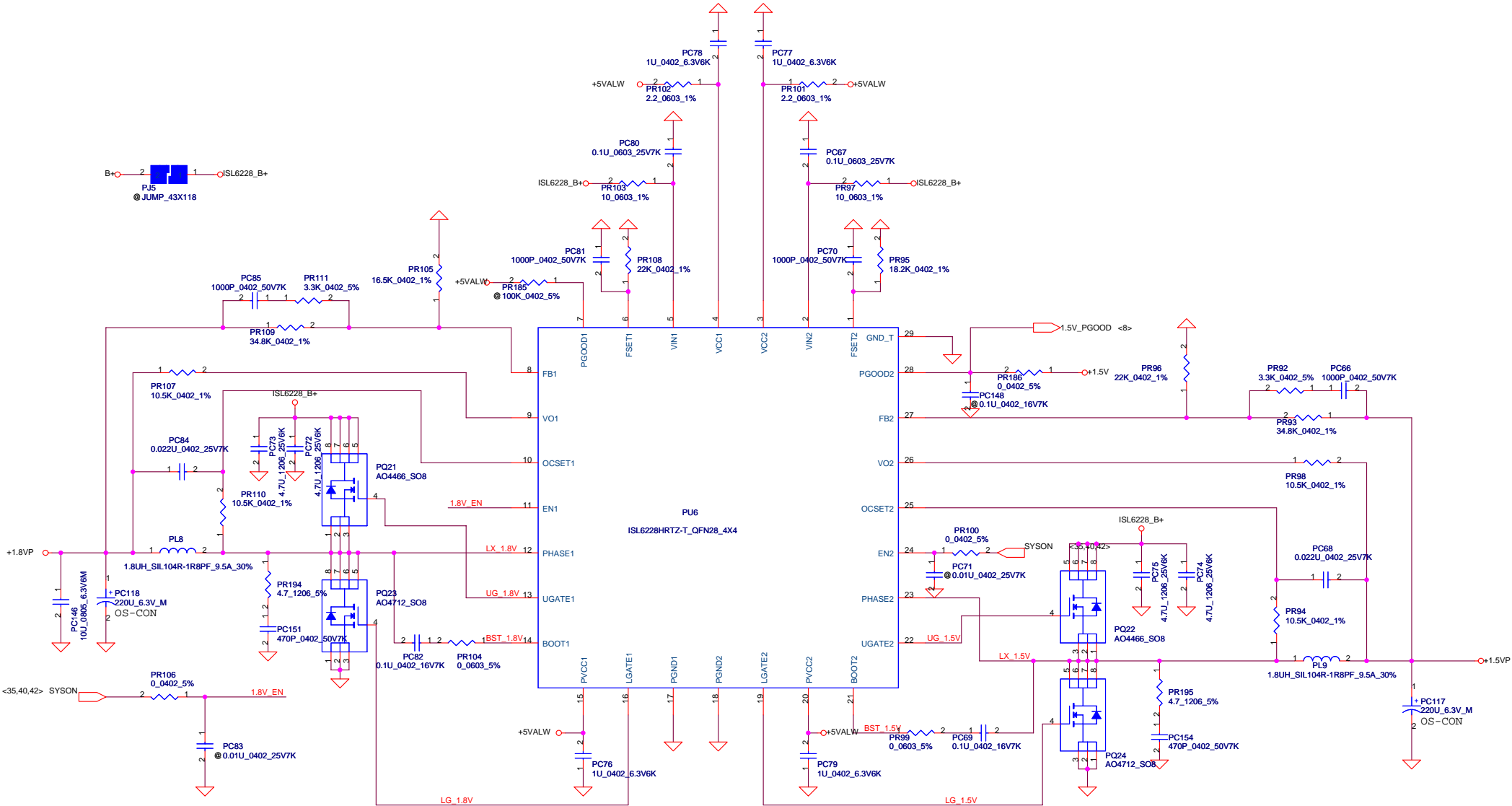
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CPU thermal protection at 92 degree C
Recovery at 56 degree C
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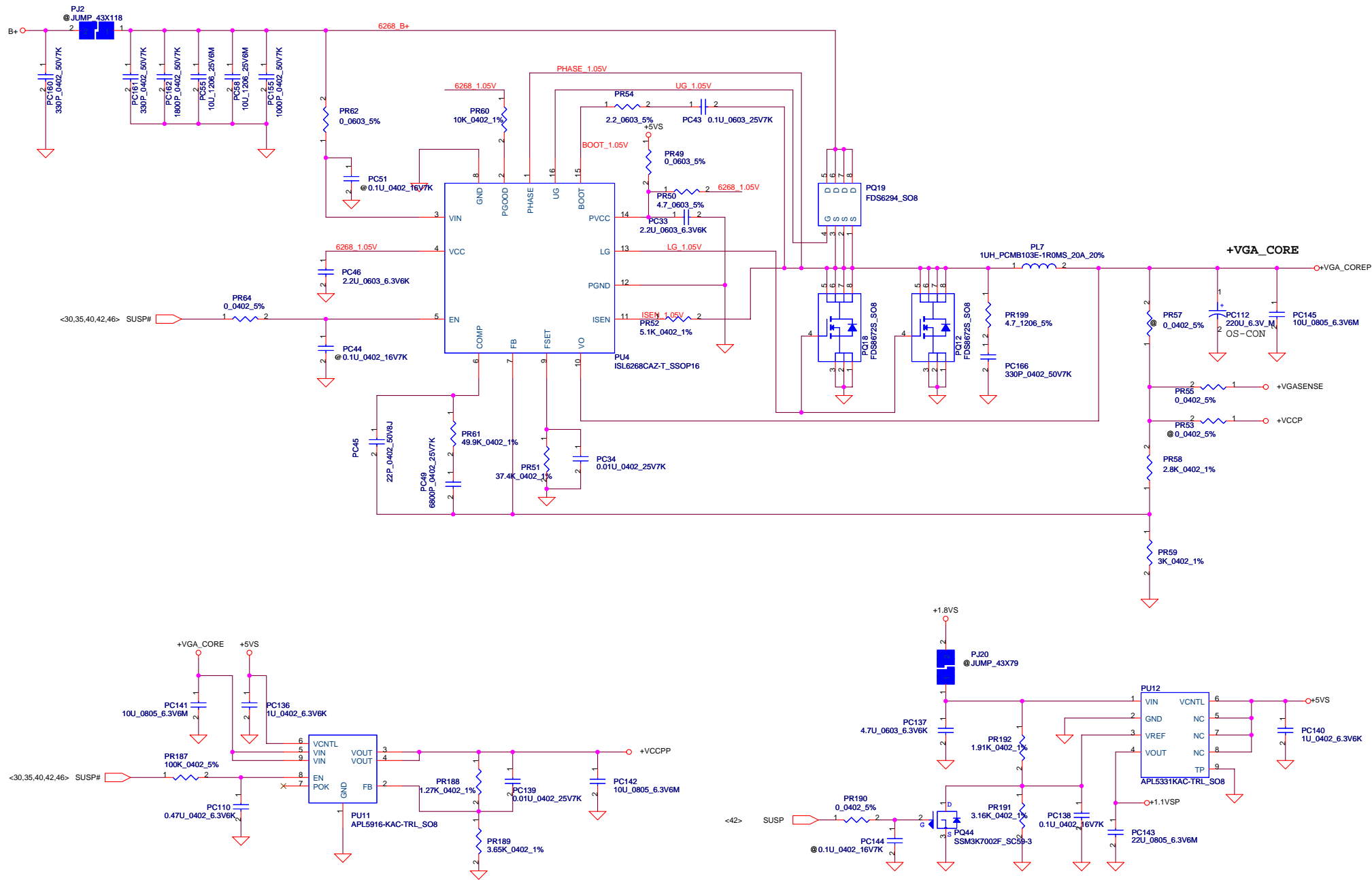


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								VGA_CORE/VCCP/1.1V			
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V
11/02		P49	Add PU12, PR190, PR191, PR192, PC137, PC138, PC140, PC143, PC144, PQ44	HW request add VCCIO(1.1V) for VGA use.
11/12		P47	Add PD16, PD17	To solve 3/5VALW reboot after remove AC.
11/21		P49	Add PC145	To reduce VGA_CORE ripple.
11/21		P49	Change PR51 from 44.4k to 37.4k.	To change VGA_CORE frequency to 350KHz
12/03		P48	Add PC146	To reduce 1.8VP ripple.
12/03		P47	Add PC147	To reserve for 3/5V IC 2nd source.
12/17		P48	Change PR105 from 16.9k_0402_1% to 16.5k_0402_1%, PR96 from 16.9k_0402_1% to 22k_0402_1%, PR93 from 25.5k_0402_1% to 34.8k_0402_1%.	Adjust 1.5V to 1.549V, 1.8V to 1.8V to 1.865V
12/17		P48	Add PC148.	Reserve for HW adjust power sequence.
12/27		P47, P48, P49, P50	Add PC149, PC150, PC152, PC153, PC155, PC151, PC154, PC156, PC157, PC158, PR194, PR195, PR196, PR197	For EMI request, to decrease power broadband.
12/31		P49	Change PR58 from 2.8k_0402_1% to 3k_0402_1% PR188 from 1.27k_0402_1% to 1.4k_0402_1%.	For intel request, ES2 NB need adjust VCCP to 1.1V.
02/29		P46	Add PR198, PC159.	Reserve charger sunbber.
02/29		P46	Change PR192 from 1.87k_0402_1% to 1.91k_0402_1%.	HW request adjust 1.1V to 1.12V.
02/29		P49	Change PR64 from 0_0402_5% to 100k_0402_1%, PC44 to 0.47u.	HW adjust power sequence.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
04/29		P50	Add PC167, PC168, PC169	For EMI request, to decrease power broadband.

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<b>Power PIR</b>						
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NO DATE		PAGE	MODIFICATION LIST	PURPOSE
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11/12	P24	Change LVDS1 & LVDS2 connect type		
11/12	P23	Change HDMI channel		
11/12	P30	Change MDC connect JP8 , Add JP24		
11/14	P16	Remove R492, R490, R489 & R491 (I2C pull- up resistor) ,Remove R66 ( HDCP)		
11/14	P16	Unstaff R486, R487, R483, R195, R192, R172, R106, R171, C116 & C183 (unused DACB & DACC)		
11/14	P17	Remove R499 (FB commend14)		
11/14	P17	Unstaff R87, R90 & C90 (FB_VREF)		
11/14	P31	MIC P/N CHANGE FROM CY000000S00 TO CYWM64P0110		
11/15	P18	Add pull down 10kohm (single LVDS signal)		
11/15	P36	Update U32 for card reader power SW (SA000024X00)		
11/22	P32	Add D24 , R526 (add WIMAX_LED# of JP22 JP23 42PIN)		
11/22	P32	delete C737,C735,708,705,C682,C681,680 (for 3G issue)		
12/05	P23	ADD R636 IN TMDS_B_HPD#		
12/11	P8	DELETE R502,R498,RR160 (DELETE DDR2 FUNCTION)		
12/11	P11	R186 CHANGE FROM 0603 TO 0805		
12/11	P28	ADD R638 CONNECT "WOL_EN" TO 3VALW		
12/17	P28	GPIO49 add 1k Ohm pulled-down resistor		
12/17	P7	REMOVE C41		
12/21	P5	U5 CHANGE FROM ADI TO SMSC (SA00001Z700)		
12/21	P10	UMA HDMI TMDS CHANGE FROM C306 TO R640 (OOHM)		
12/21	P16	ADD External Spread Spectrum (ADD U3,R55,C66,R48;DEL R99,R100)		
12/26	P30	ADD R653,R654 TO EXTERNAL MIC		
12/27	P43	CHANGE KILL SW POWER FOR +3VS TO +3VALW		
12/31	P16	UPDATE VGA_HDMI_SCL,VGA_HDMI_SDA FROM I2CD TO I2CE		
2/13	P8	CHANGE R147 FROM 511ohm TO 499ohm 1%		
2/13	P23	CHANGE THE D4 LOCATION		
2/13	P23	ADD D25,D26		
2/13	P25	ADD D27,D28,D29		
2/14	P38	CHANGE LED		
2/14	P29	CHANGE R558,R582 FROM 10ohm TO 100ohm		
2/14	P29	CHANGE C728,C738 FROM 0.1uF TO 0.1uF		
2/14	P32	JP22,JP23 PIN37,PIN43 CONNECT TO GROUND		
2/14	P23	DELETE LEVEL SHIFT CIRCUIT		
2/14	P23	ADD R659		
3/3	P10	REMOVE R240,R235 (GHCH_CRT_HSYNC,GHCH_CRT_VSYNC)		
3/3	P11	REMOVE R186 (+VCCP_PEG)		
3/3	P11	+1.5VS_TVDAC PULL DOWN		
3/3	P28	TO USE THE RSMRST CIRCUIT		
3/3	P28	ADD C804,C805,C806,C807 (ESD REQUESTION)		
3/17	P16	CHANGE R69,R71 FROM 10Kohm TO 2.2Kohm		
4/18	P36	change L41,L42 from L to 0ohm		
5/2	P5	ADD R667,C810 FOR FAN solution RC (R=1Kohm,C=10nF)		
5/2	P30	ADD R668,C811,R669 FOR MIC solution RC (R=1Kohm,C=10uF) , INT_MIC CONNECT TO U15 PIN23		
5/2	P42	ADD R670,R671,R672 FOR AO4468 VGS ISSUE solution		

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